

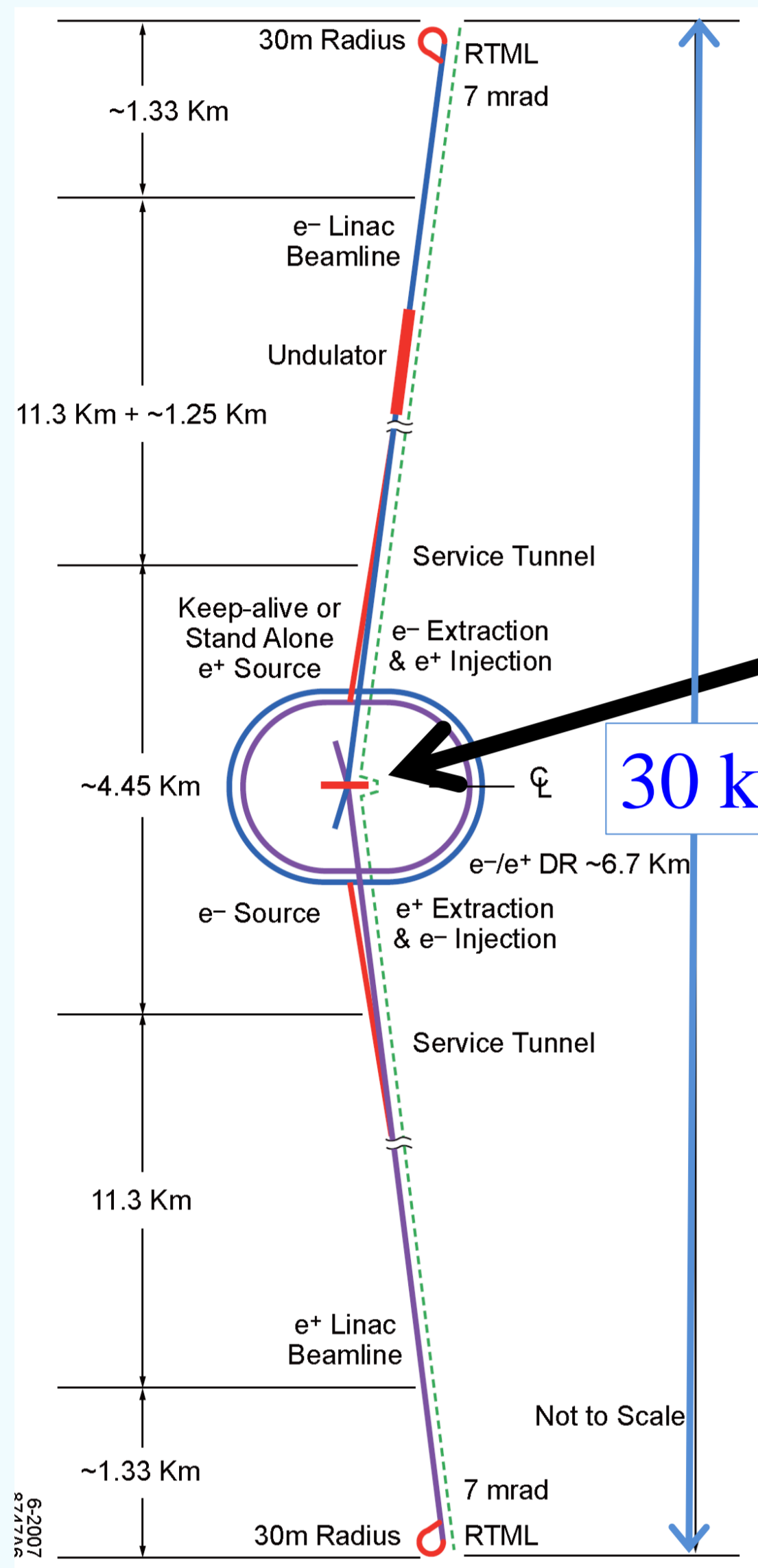
Tomoyuki Saito (Physics, Tohoku Univ.)

## What is ILC?

ILC (International Linear Collider) is planned for the next generation of the high energy frontier physics.

### ILC accelerator

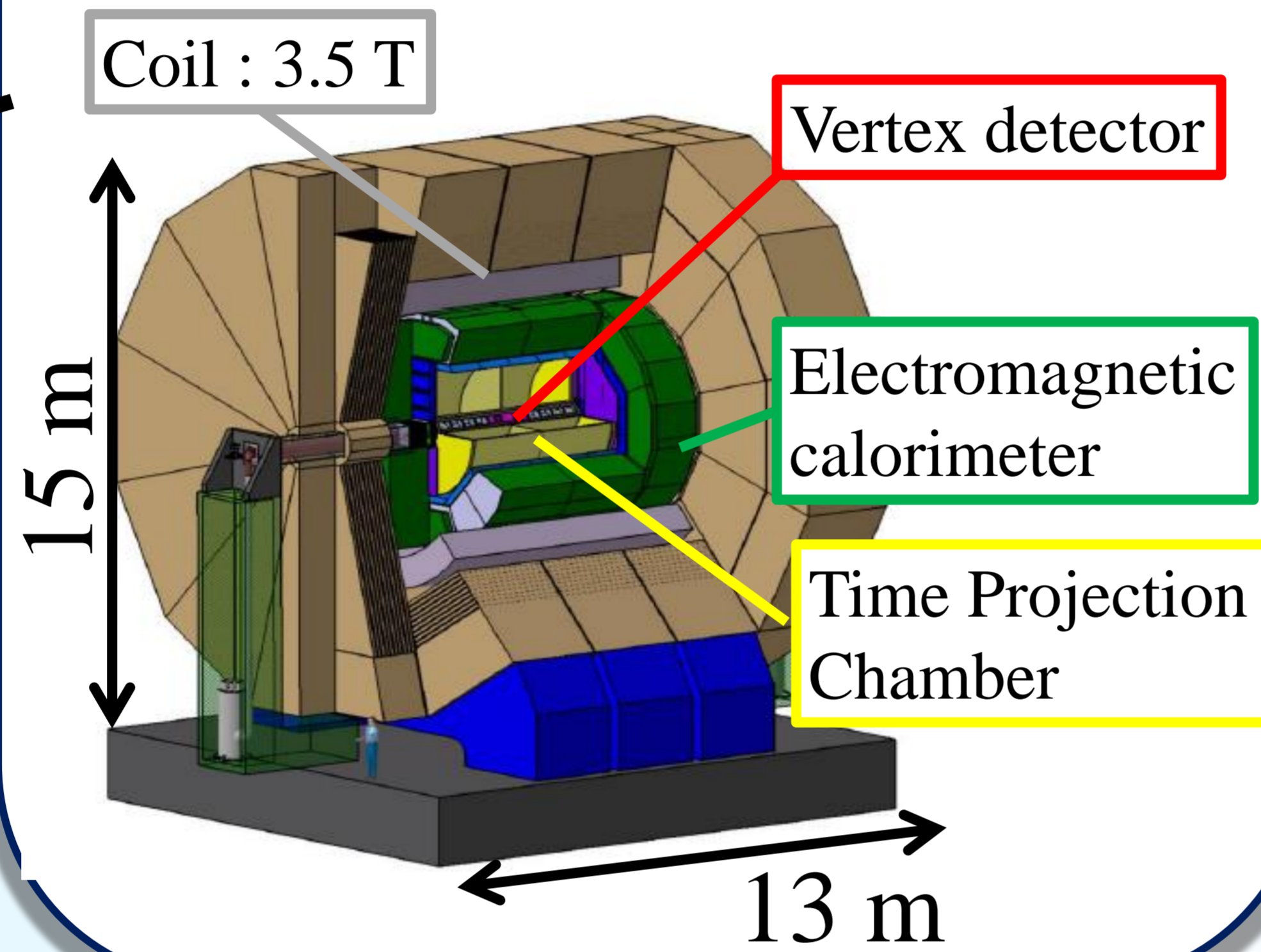
Electrons and positrons are accelerated along the linear accelerator in 30 km long underground tunnel.



### Detector

The role of the detector is to measure precisely the information on the particles from the collision.

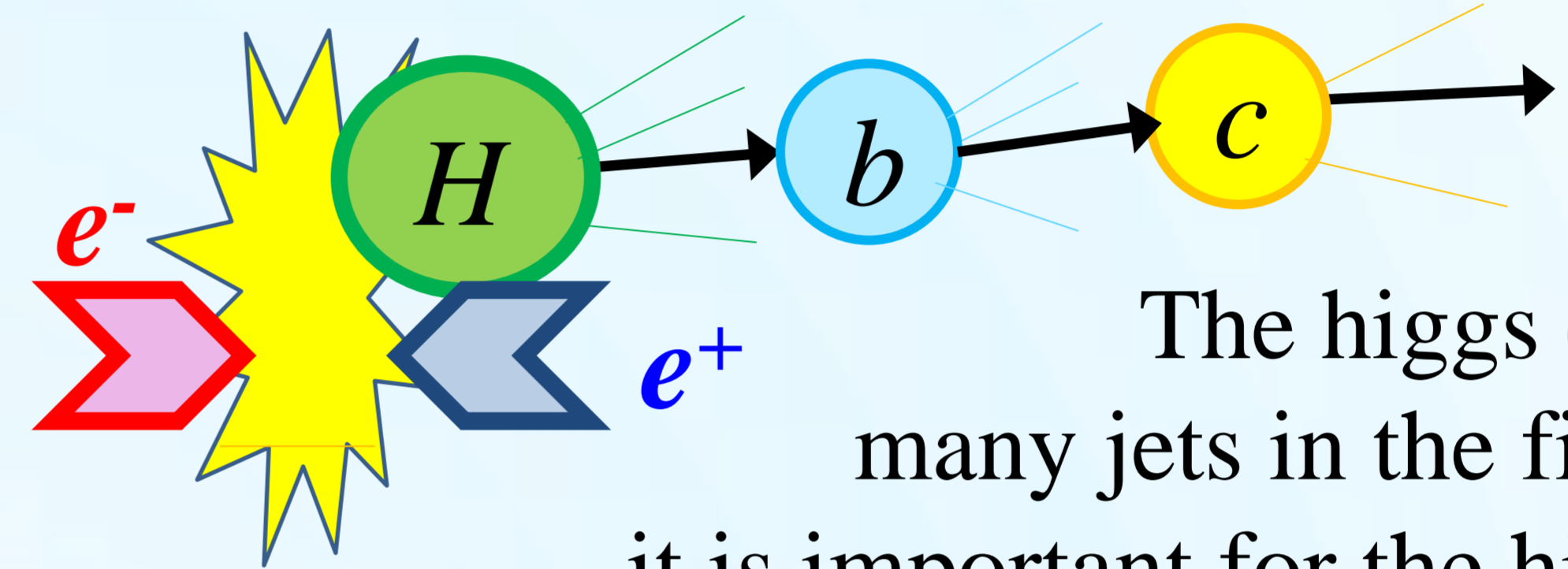
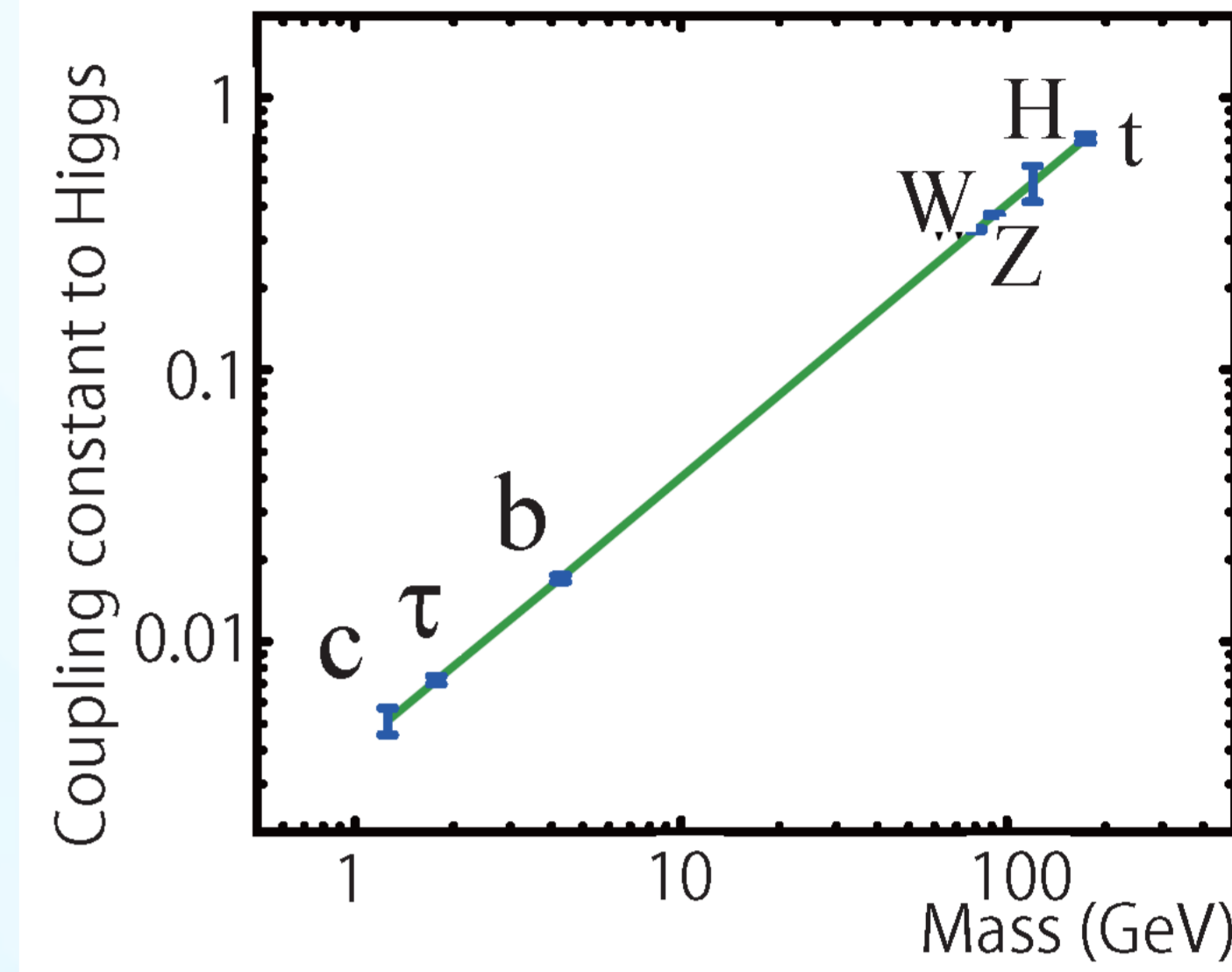
- Interaction point : Vertex detector
- Momentum : Time Projection Chamber
- Energy : Calorimeter



### ILC Physics : Higgs study

#### Higgs mechanism

In higgs mechanism, the coupling constants to higgs boson of particles are proportional to the masses.



The higgs event has the many jets in the final state. So, it is important for the higgs study to identify the origin of these jets. So, the excellent performance of event reconstruction is requested to the detector, especially **the vertex detector**.

$$\text{Impact parameter resolution: } \sigma = 5 \oplus \frac{10}{p\beta \sin^{3/2} \theta} (\mu\text{m})$$

## Development of FPCCD vertex detector

### What is the FPCCD vertex detector?

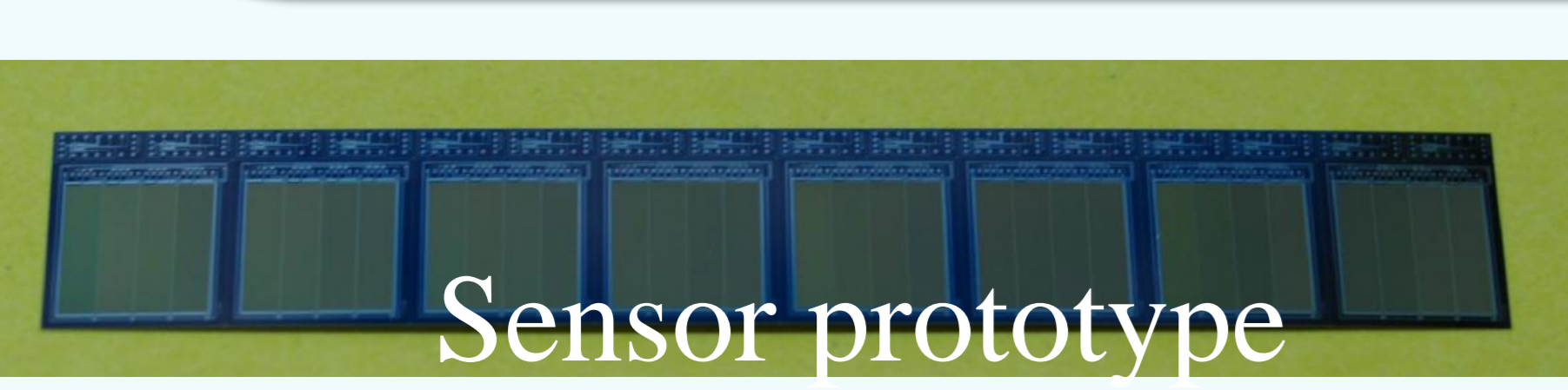
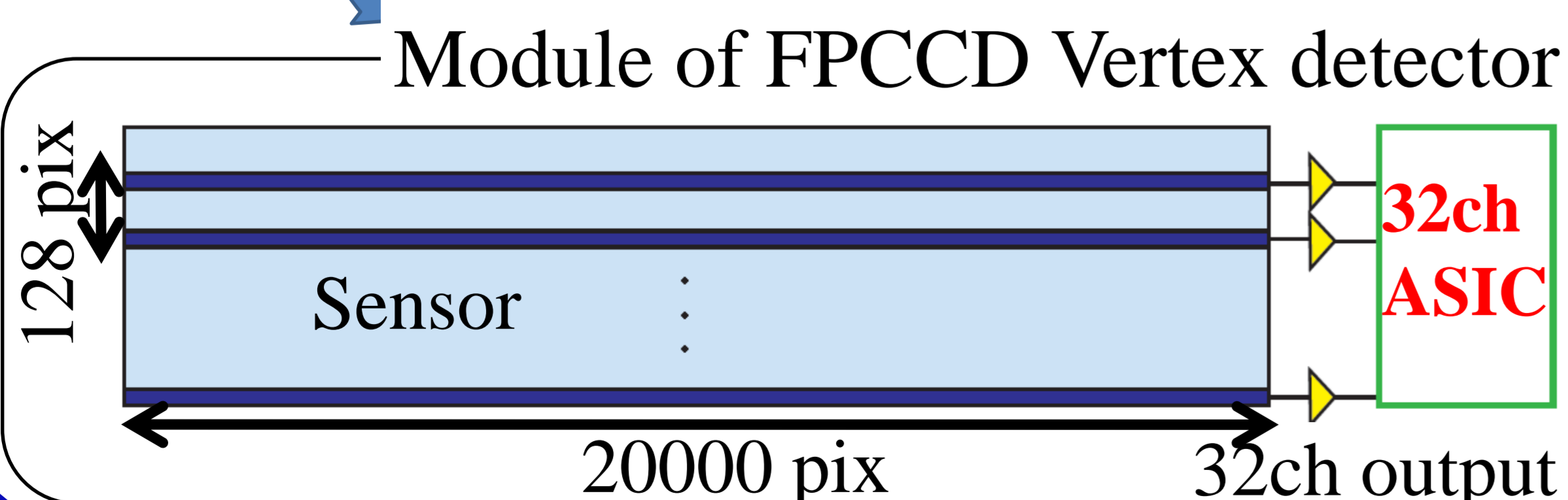
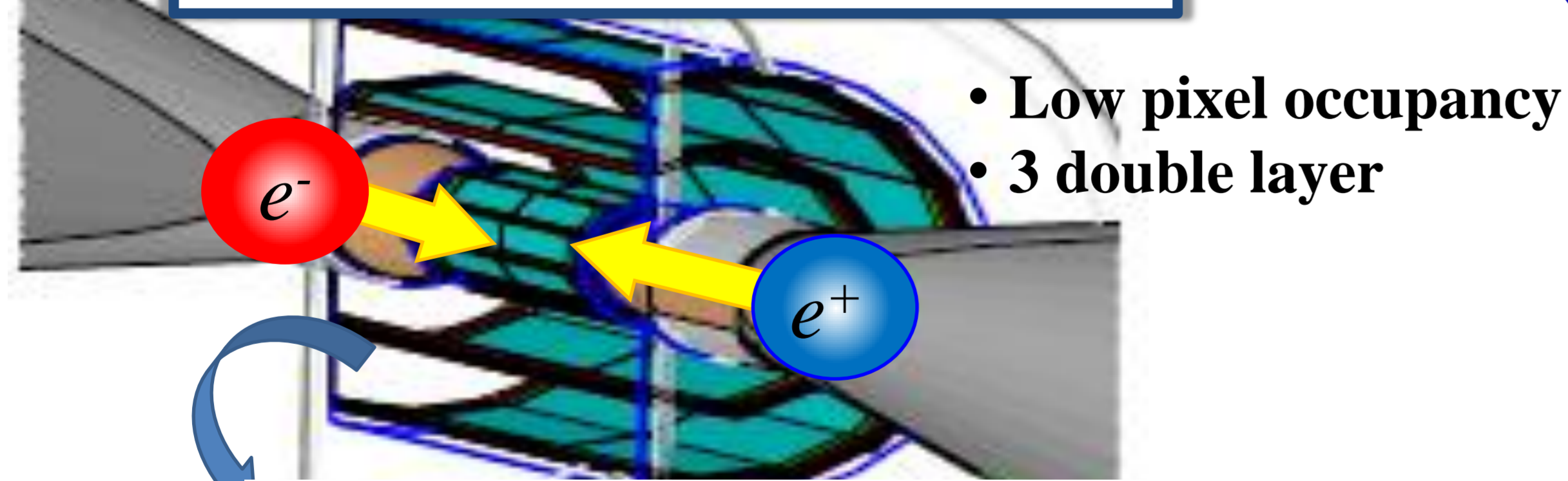
FPCCD VTX has the fine-pixel CCD sensor and can realize the precise measurement on the decay point.

- Pixel size :  $5\mu\text{m} \times 5\mu\text{m}$  (20000  $\times$  128 pix/sensor)
- Sensitive region :  $15\mu\text{m}$  (Full-depleted)
- Multi-channel (32ch/sensor)

- Number of total channel : 6080 **Very large!**
- Number of total pixel :  $10^{10}$

It is essential to develop multi-channel readout ASIC.

### FPCCD vertex detector

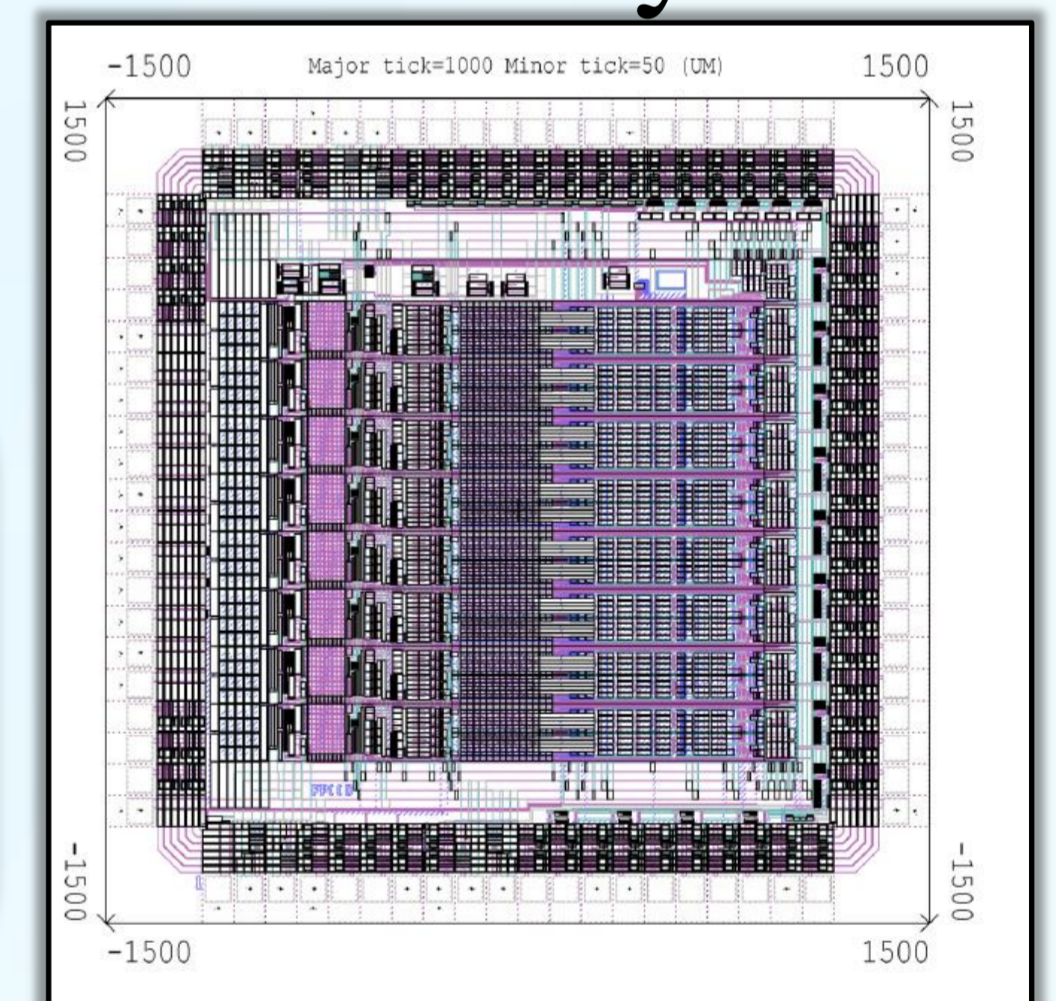


### Readout ASIC

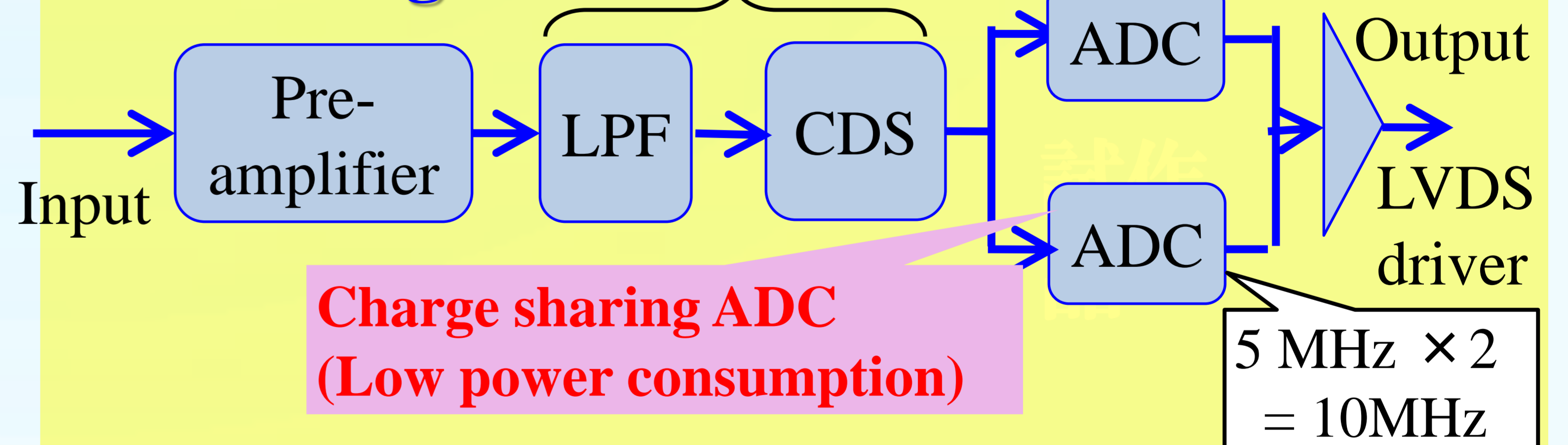
#### Requirements for ASIC

- Readout speed > 10 MHz
- Noise level < 30 electron
- Power Consumption < 6 mW/ch

#### ASIC layout



#### ASIC design Noise suppression



Charge sharing ADC (Low power consumption)

$$5 \text{ MHz} \times 2 = 10 \text{ MHz}$$

The ASIC can be almost satisfied with the requirements on the readout speed and noise level, but not on the power consumption (27 mW/ch).

ASIC design study has been continued.

