Development of Readout ASIC for FPCCD Vertex Detector

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Outline

- FPCCD Vertex detector
- Readout ASIC for FPCCD
- Performance of ASIC
- FPCCD readout test
- Second prototype
- Summary

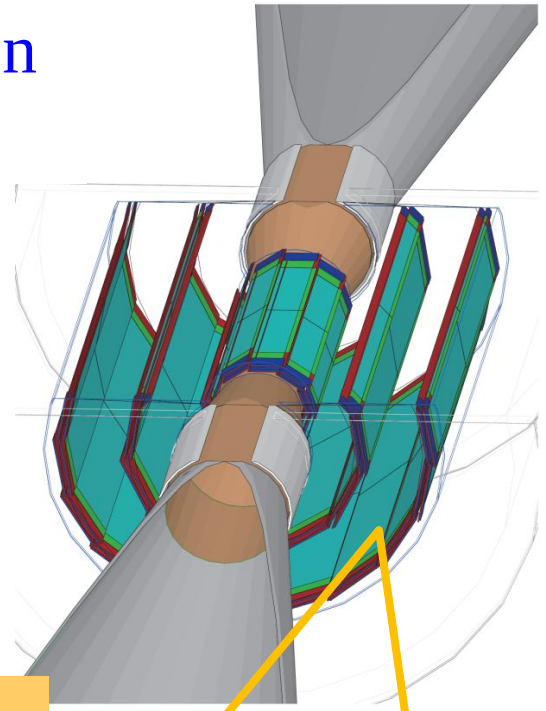
FPCCD Vertex detector

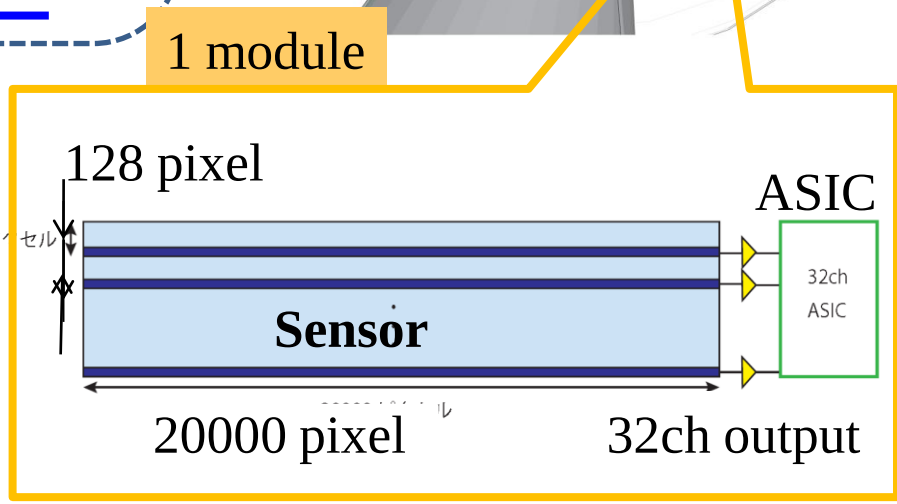
FPCCD VTX can realize the good resolution and low pixel occupancy.

- Pixel size : **5 μm×5 μm**
- Sensitive thickness :15μm(Full-depleted)
- Multi-channel CCD sensor (32ch)
- Total number of channel : 6080
  - 20000×128 pix/ch

  ⇒ **Total number of pixel ～10^{10}**

It is important to establish the readout system.



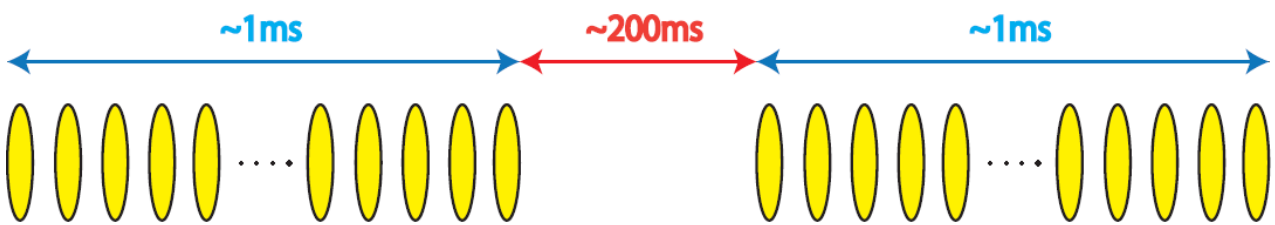


Development of Readout ASIC

We have to develop **the multi-channel middle-speed readout** ASIC with **low power consumption**.

Challenging requirements for ASIC

- Readout speed > 10 MHz



1 train ~ 2650 bunch

Development of Readout ASIC

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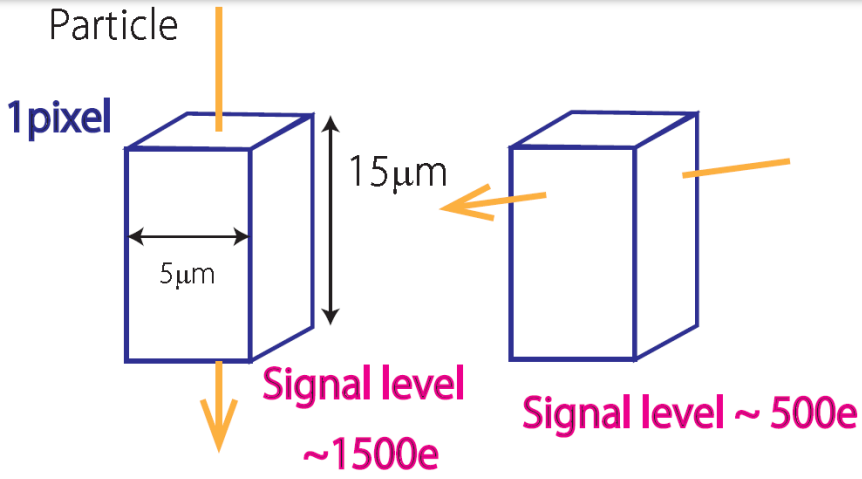
Challenging requirements for ASIC

- Readout speed > 10 MHz
- Noise level < 30 electrons



Development of Readout ASIC

We have to develop **the multi-channel middle-speed readout** ASIC with **low power consumption**.

Challenging requirements for ASIC

- Readout speed > 10 MHz
- Noise level < 30 electron
- Power Consumption < 6 mW/ch

Particle

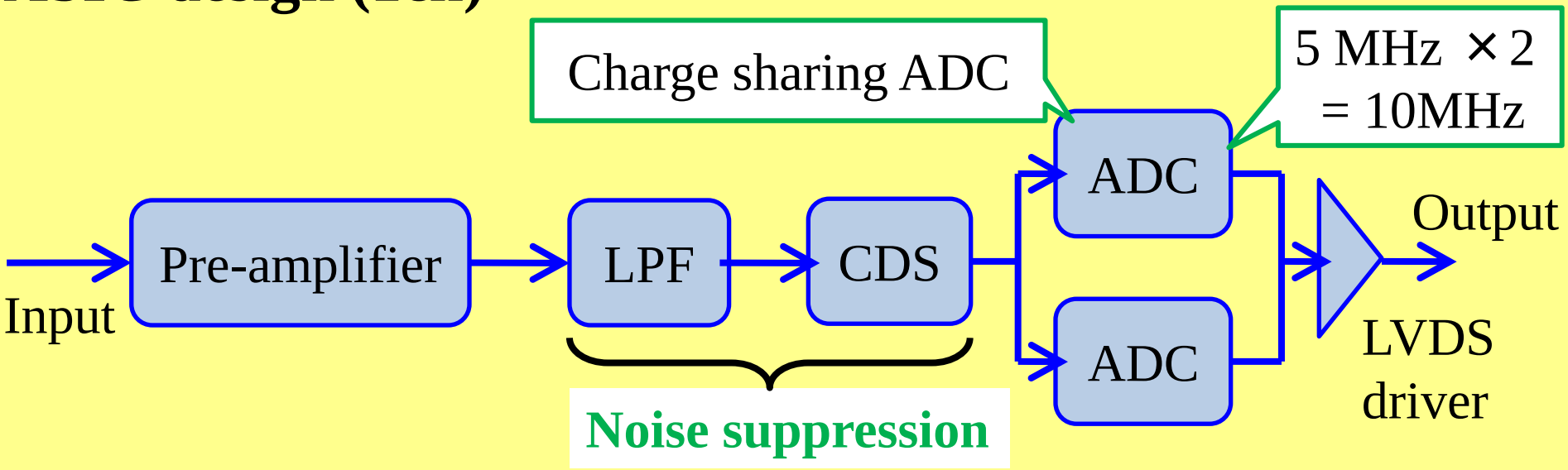
We designed the ASIC satisfied about these requirements.

~1500e

Signal level ~ 500e

Design of Readout ASIC

ASIC design (1ch)



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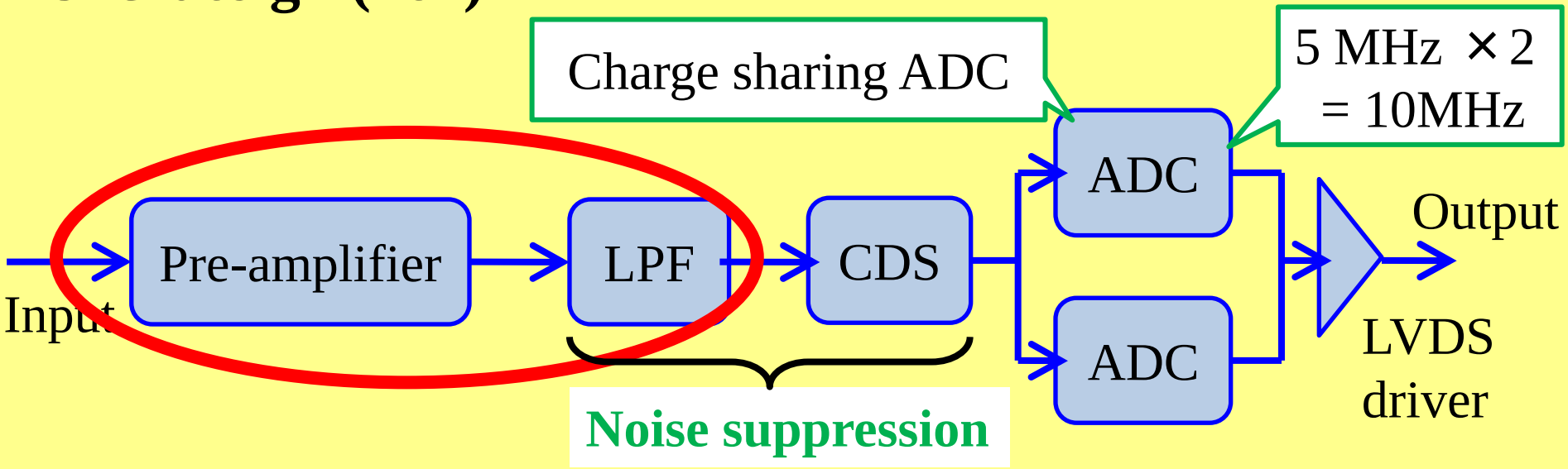
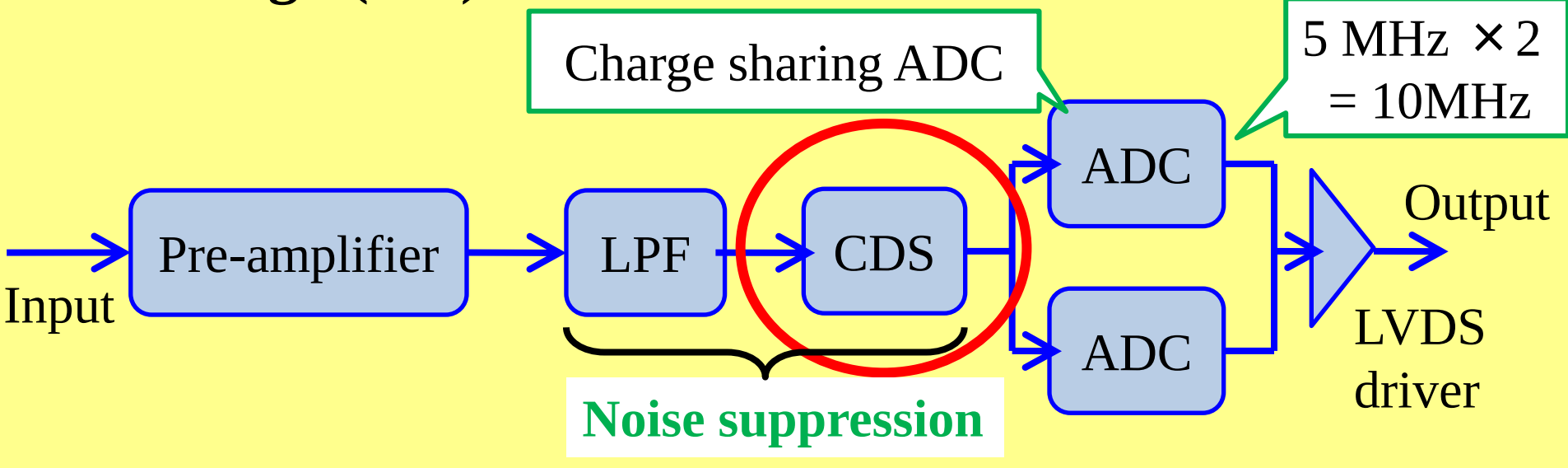


- **The parameters** of Pre-amplifier and Low-pass filter (LPF) **can be set along the command by PC.**

Design of Readout ASIC

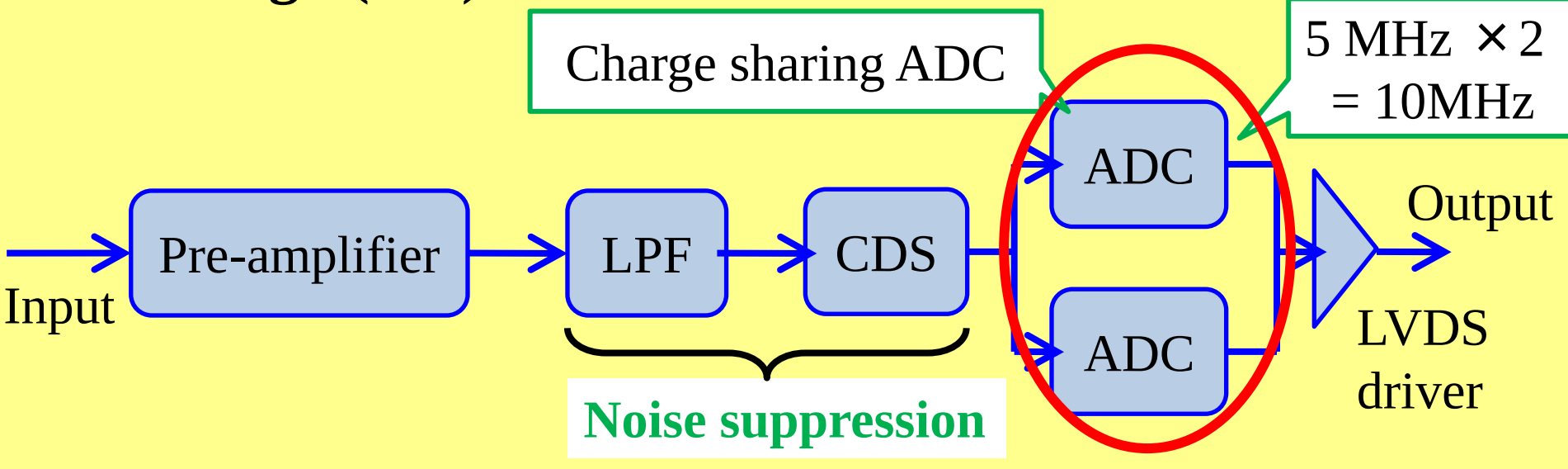
ASIC design (1ch)



- **The parameters** of Pre-amplifier and Low-pass filter (LPF) **can be set along the command by PC.**
- Correlated Double Sampling (CDS) works effectively to suppress **the noise on CCD**.

Design of Readout ASIC

ASIC design (1ch)

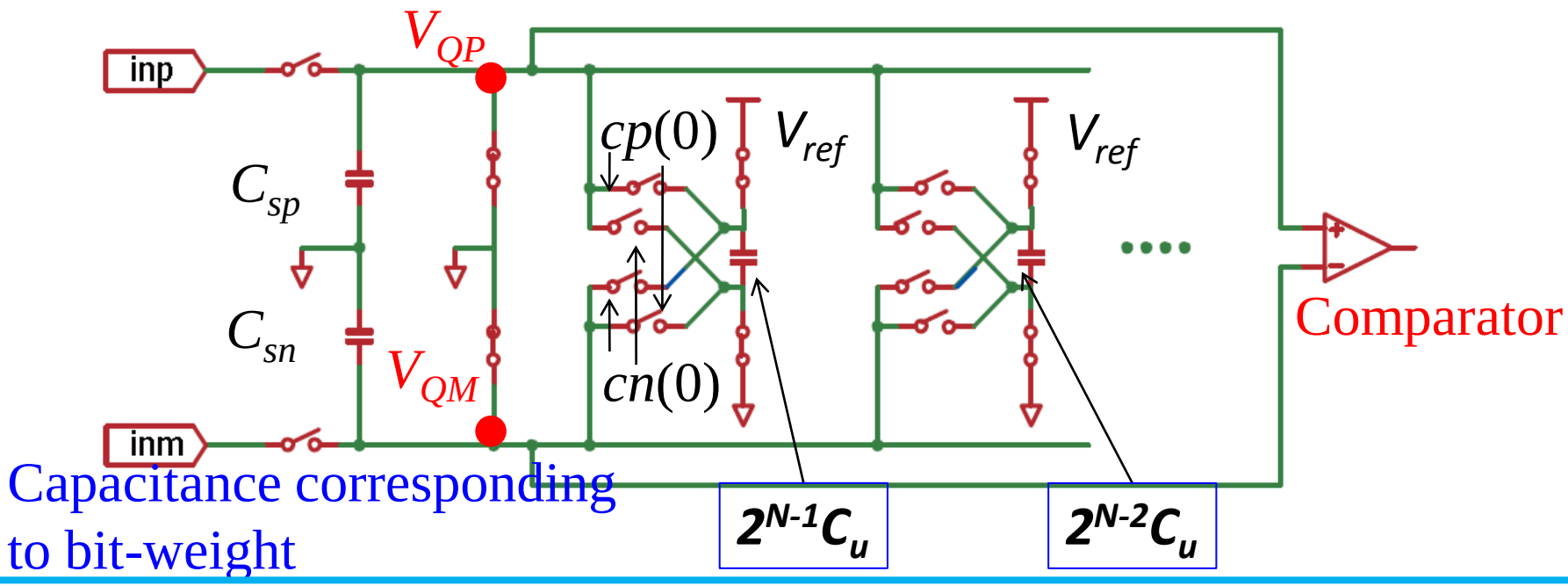


- **The parameters** of Pre-amplifier and Low-pass filter (LPF) **can be set along the command by PC.**
- Correlated Double Sampling (CDS) works effectively to suppress **the noise on CCD**.
- **Charge sharing ADC** has **low power consumption.**

Charge sharing ADC

Charge sharing ADC：Low power consumption

A/D conversion by the charge operation between capacitance array



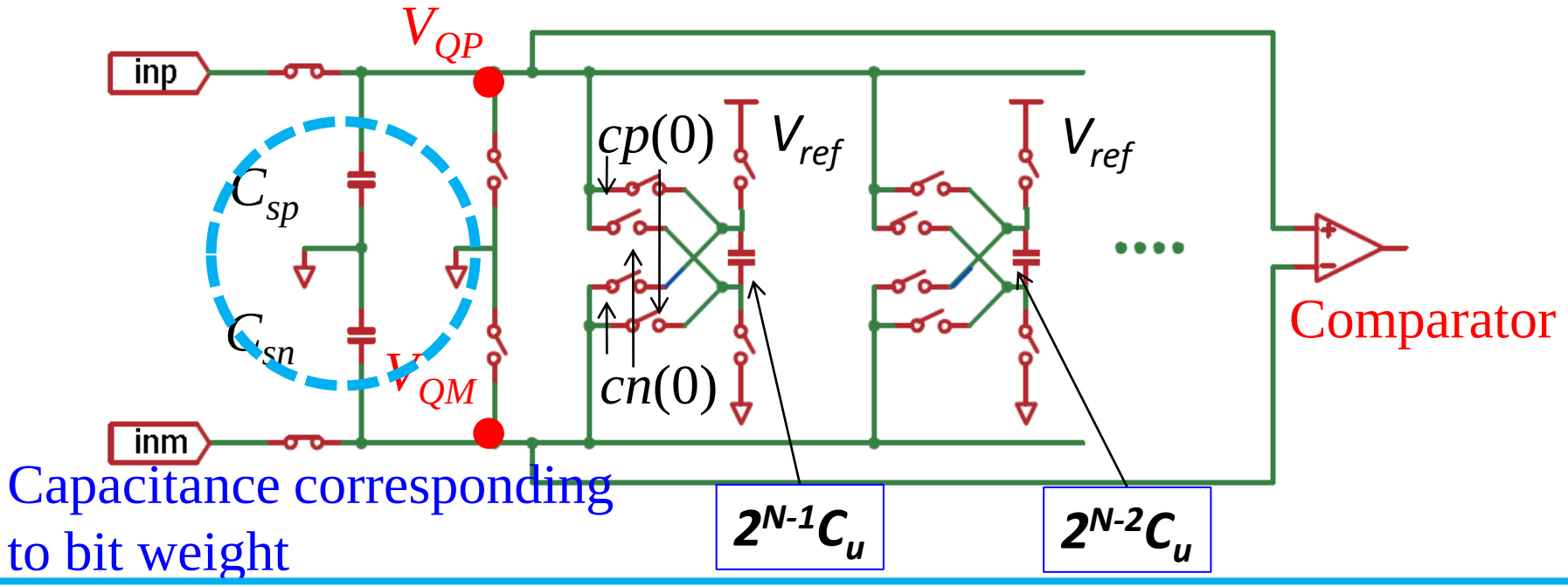
Capacitance corresponding to bit-weight

Charge sharing ADC

Charge sharing ADC：Low power consumption

A/D conversion by the charge operation between capacitance array

① Input signal is accumulated at C_{sp} and C_{sn}, and the comparator compares V_{QP} and V_{QM}. → **decision on the highest-bit**



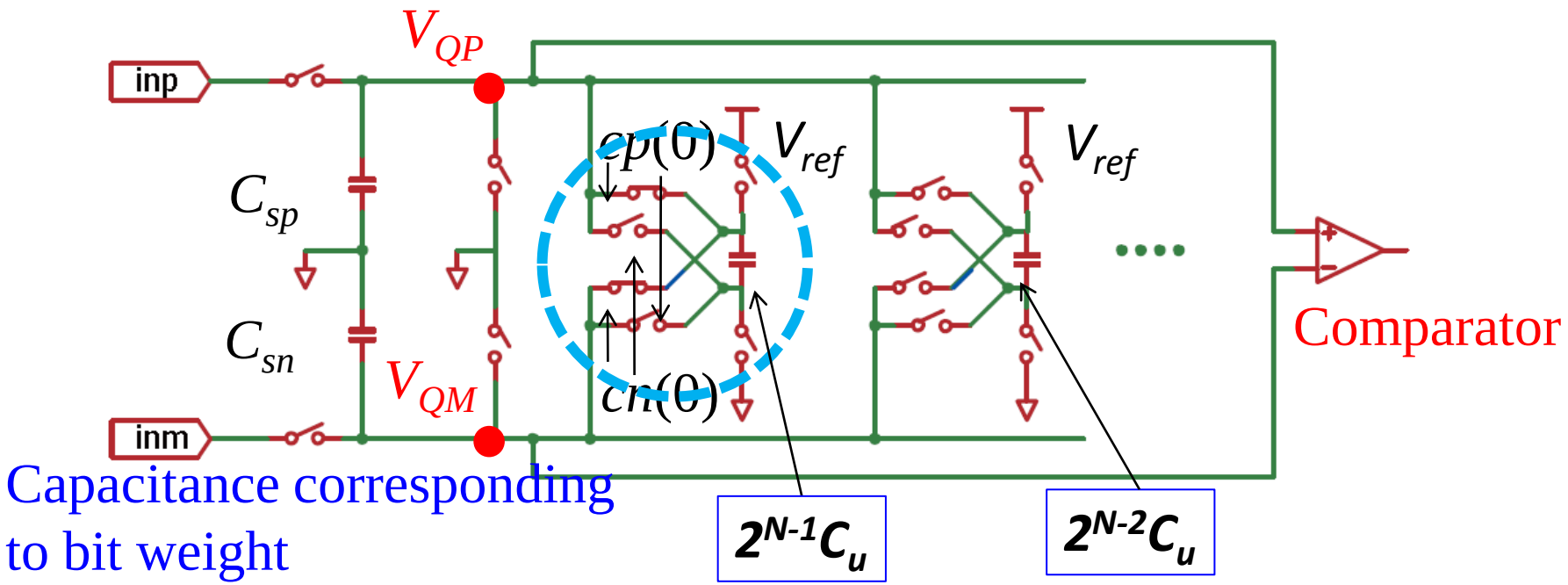
Charge sharing ADC

Charge sharing ADC：Low power consumption

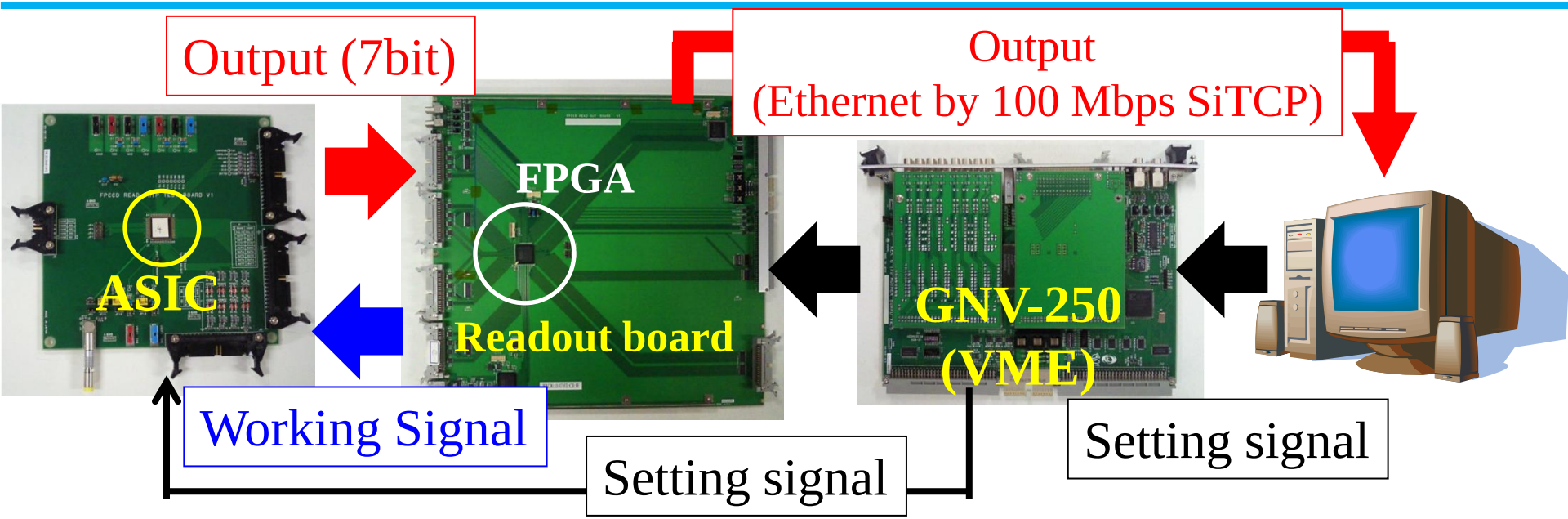
A/D conversion by the charge operation between capacitance array

① Input signal is accumulated at C_{sp} and C_{sn}, and the comparator compares V_{QP} and V_{QM}. → **decision on the highest-bit**

② Switch *cp* or *cn* (depend on the result of ①) is connected.
→ compare V_{QP} and V_{QM} → **decision on second-bit**



ASIC readout system



Component

- **Board for ASIC**
- **Readout board** (equipped for the main FPGA)
  → Clock production, Sending the working signal
- **GNV-250 (VME)** → Setting of the parameter (Gain, LPF)
- **PC** → Software process (DAQ-Middleware)

The performance of ASIC was tested by the developed system.

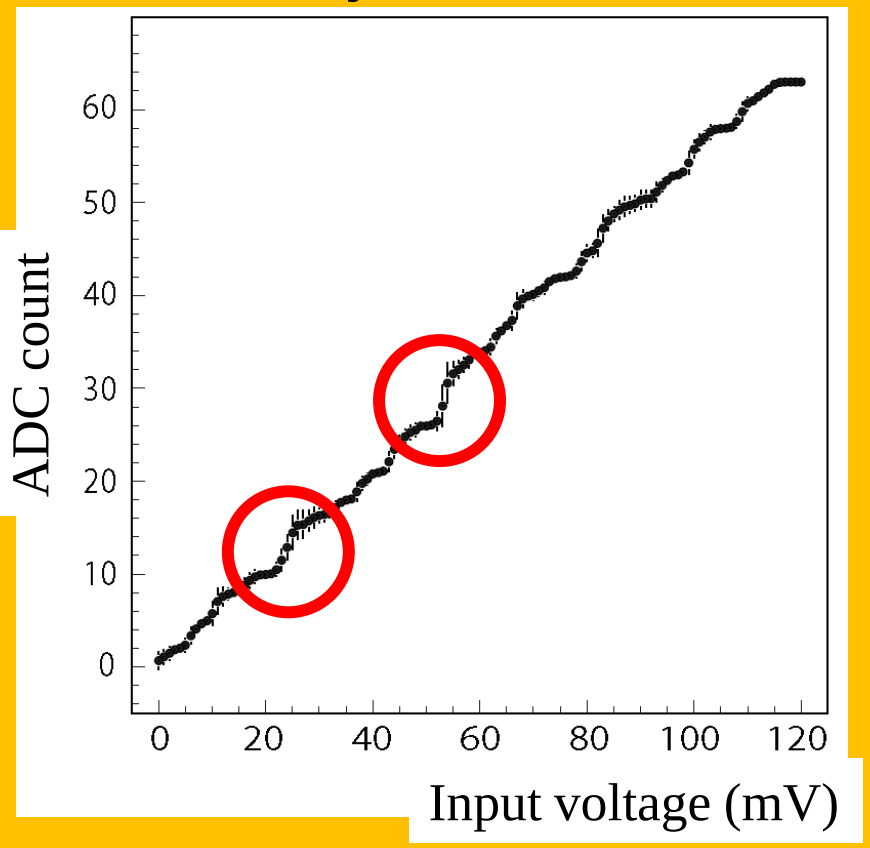
Performance test of 1st prototype ASIC

The results on the performance test are summarized.

	Result	Goal	Status
Readout speed	1.5 MHz	10 MHz	▪ **Lack of current** to ADC at high speed readout ▪ Effect on the **stray capacitances**
Noise level	40 e	30 e	▪ 1ADC count=40e ← too big ▪ Some ADC counts are missing
Power consumption	13 mW/ch (Simulation)	6 mW/ch	Analog and digital parts are same

Performance test of 1st prototype ASIC

Linearity measurement



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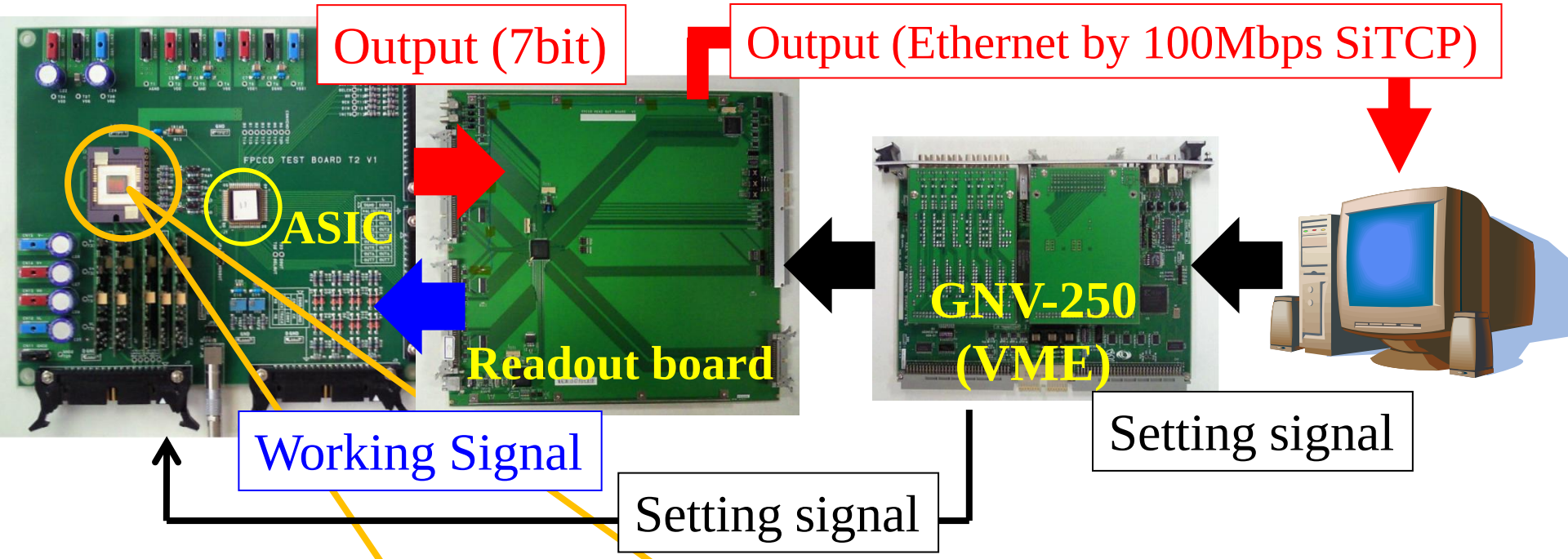
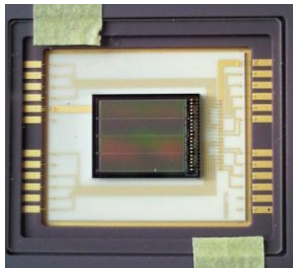
We have to address these issues in next prototype of ASIC.

FPCCD readout

FPCCD readout system

The readout test of FPCCD was performed by the developed system.





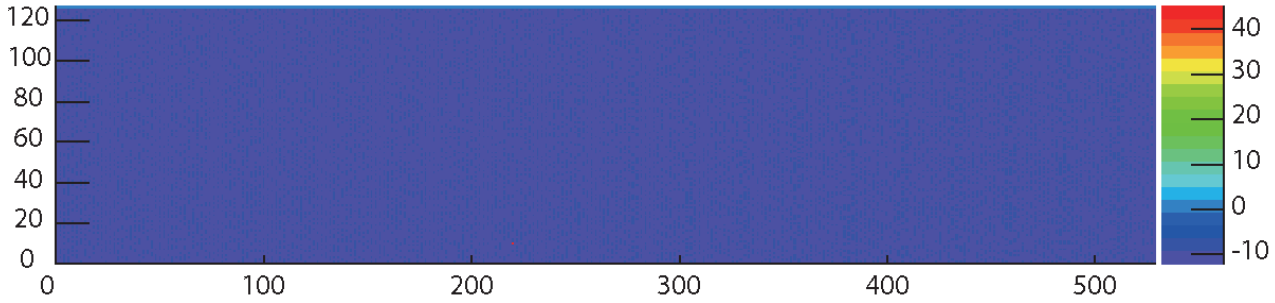
FPCCD prototype (by Hamamatsu)

- Pixel size : 12 μm×12 μm
- Number of channel : 4

FPCCD readout test

The signal which was sent from FPCCD to the PC is investigates.

Pedestal distribution (ADC count)



⇒ **Uniform distribution**

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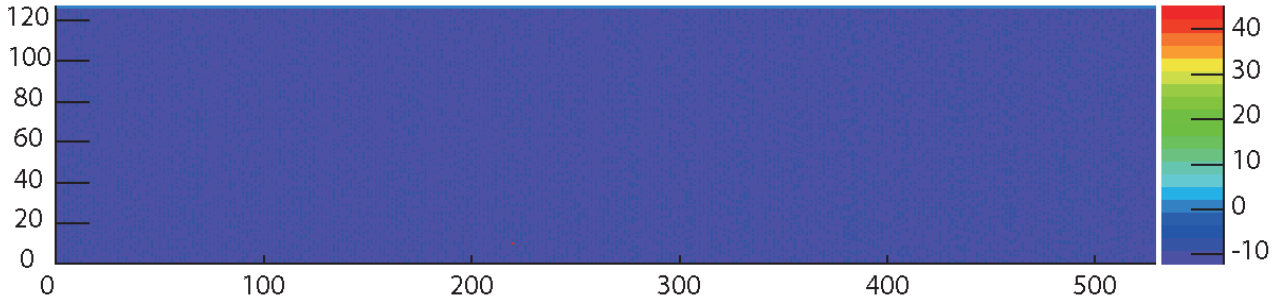
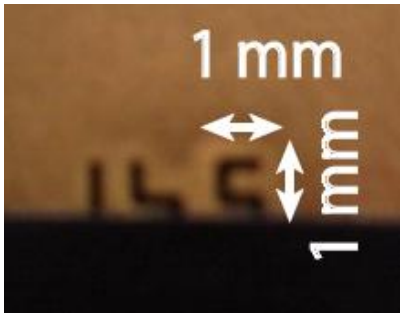
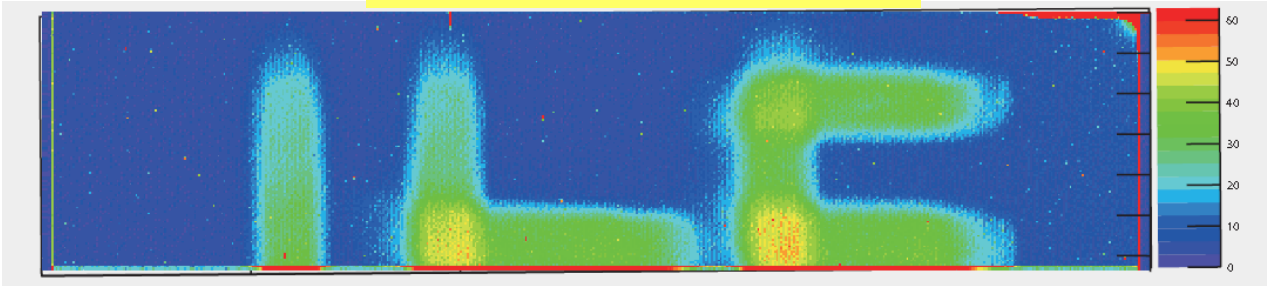


⇒ **Uniform distribution**

Photomask



LED irradiation test



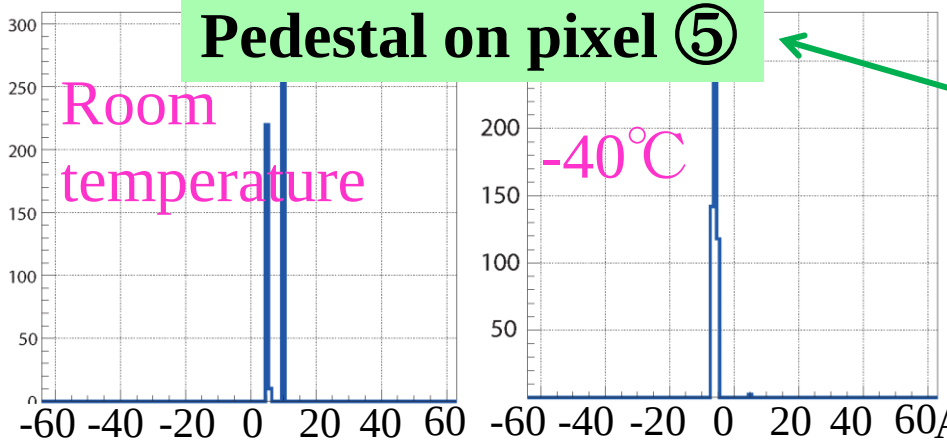
Success in reading “ILC”

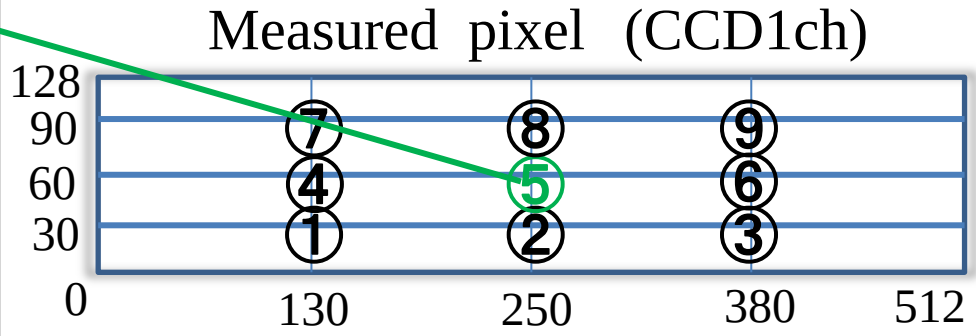
The developed readout system works normally.

Readout noise on total system

The pedestals on each pixels are checked to estimate the total noise (Requirement : 50e).

Pedestal on pixel ⑤





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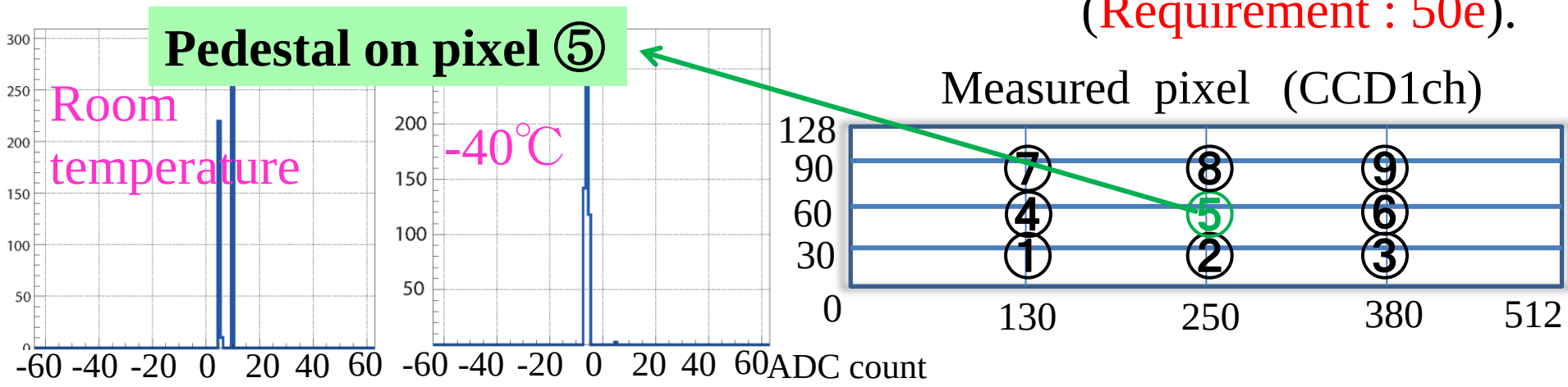

Noise on each pixel (electron)

Pixel	①	②	③	④	⑤	⑥	⑦	⑧	⑨	Ave.
Room temperature	100	72	96	92	100	100	96	68	92	91
-40℃	38	30	44	48	48	40	40	34	40	40

- The noises at -40℃
  - equal to that of only ASIC.
  - are satisfied with the requirement (50 electrons).

Development of 2nd prototype ASIC

Problems on the 1st prototype ASIC

① Slow readout speed
② Big jumps on ADC count output by the stray capacitances
③ Large power consumption

Development of 2nd prototype ASIC

Goal：10 MHz readout speed and solution to ADC count jumps

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Main modification

- Readout speed : The number of pins is increased, 80 → 100.

Development of 2nd prototype ASIC

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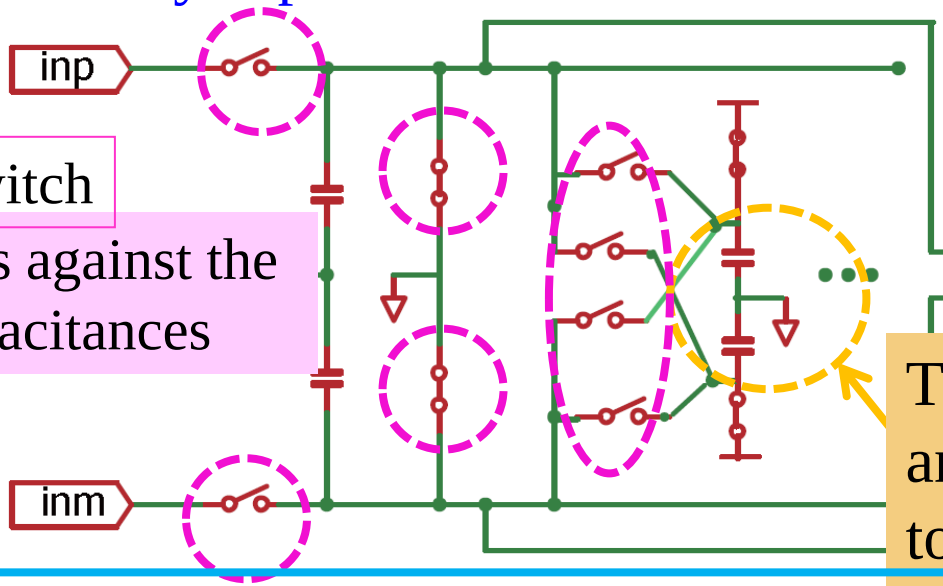
- Readout speed : The number of pins is increased, 80 → 100.
- Some jumps of ADC counts
  - Addition the offset adjustment circuit to the comparator.

Development of 2nd prototype ASIC

Goal：10 MHz readout speed and solution to ADC count jumps

Main modification

- Readout speed : The number of pins is increased, 80 → 100.
- Some jumps of ADC counts
  - Addition the offset adjustment circuit to the comparator.
  - Change of the ADC design for the suppression of the effect on the stray capacitance



Switch

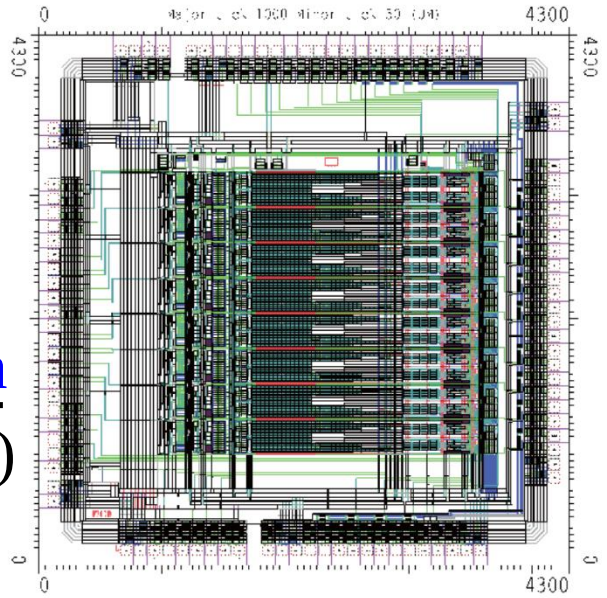
Measures against the stray capacitances

Comparator

Bit- weight capacitance

The capacitance is divided and the bases are connected to the earth.

Performance test by Post layout simulation

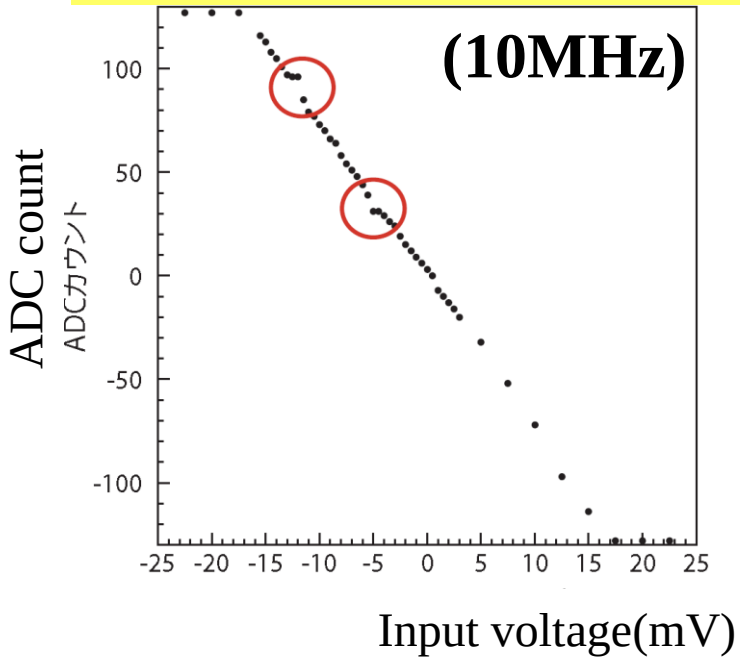


The layout is designed by Digian Technology.

⇒ Performance test by the post layout simulation

(simulation by the data from layout)

Linearity measurement



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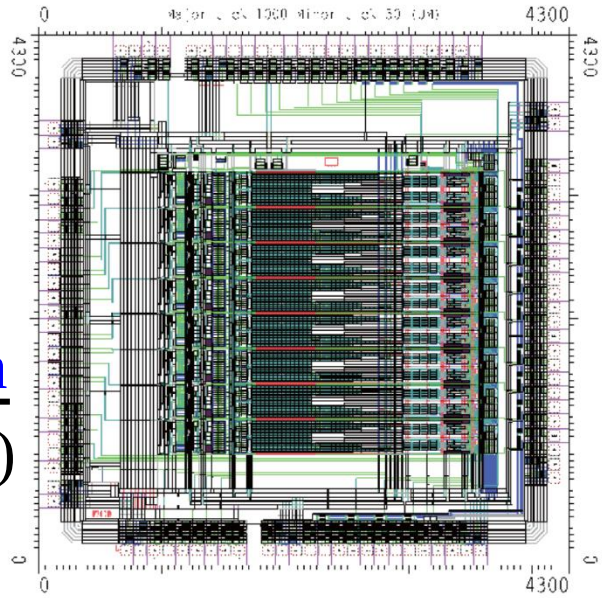

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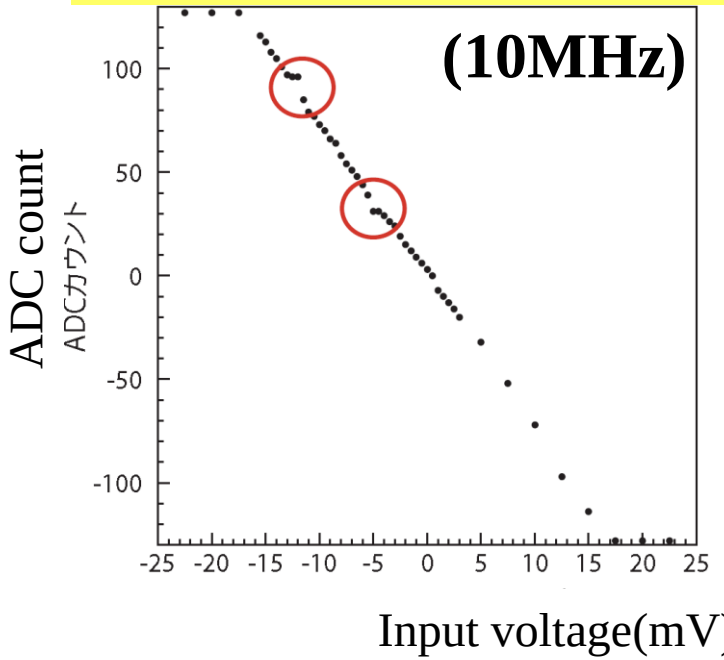
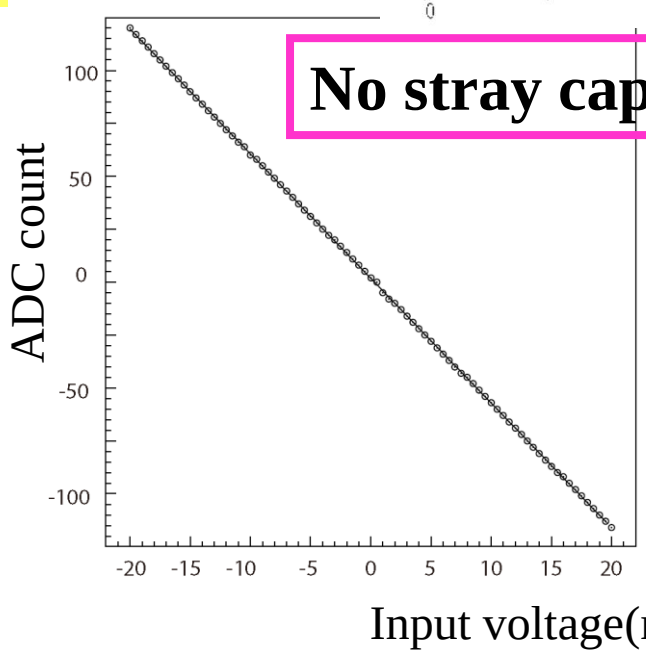




No stray capacitance

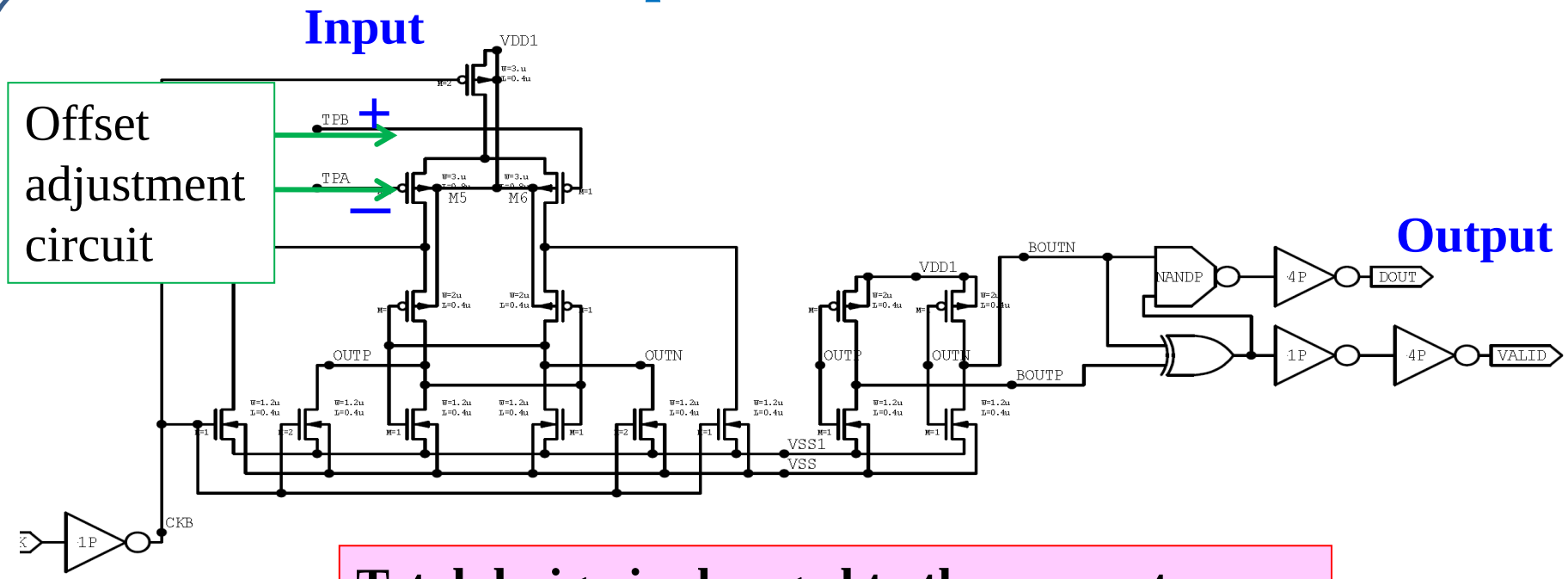
Some ADC counts are still missing because of **the stray capacitance in the comparator.**

Development of 2nd ASIC ②

More modification

- ADC count jump : Change on the design of the comparator
  - Suppress the effect on the stray capacitance

New comparator circuit in ADC



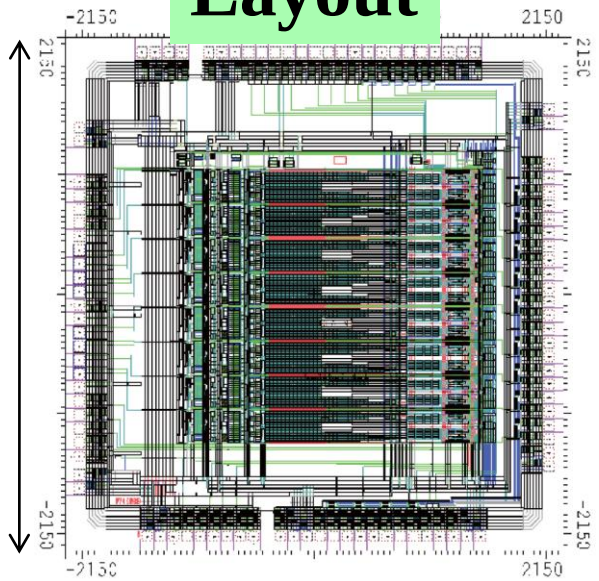
Total design is changed to the symmetry one

Performance test ② by Post layout simulation

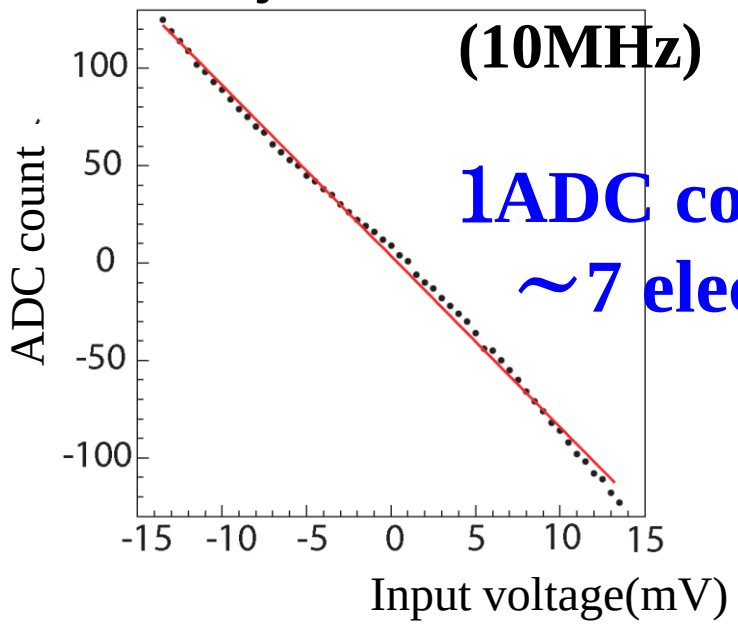
The layout added more changes was also designed by Digian Technology.

⇒ Performance test by the post layout simulation

Layout



Linearity measurement (10MHz)



1ADC count ～7 electron

The design of the second ASIC works normally at 10 MHz

The 2nd prototype ASIC arrived at the end of Feb.

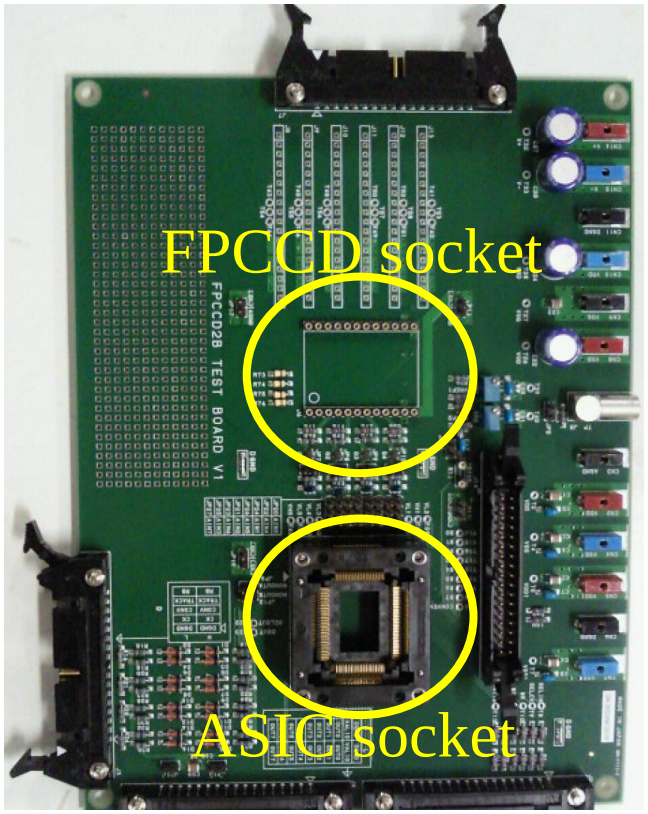
2nd prototype of ASIC

2nd prototype ASIC

- Produced by TSMC
- Process：0.35μm CMOS
- Number of channel：8
- Chip area size：4.3 mm×4.3 mm

2nd prototype ASIC packaged

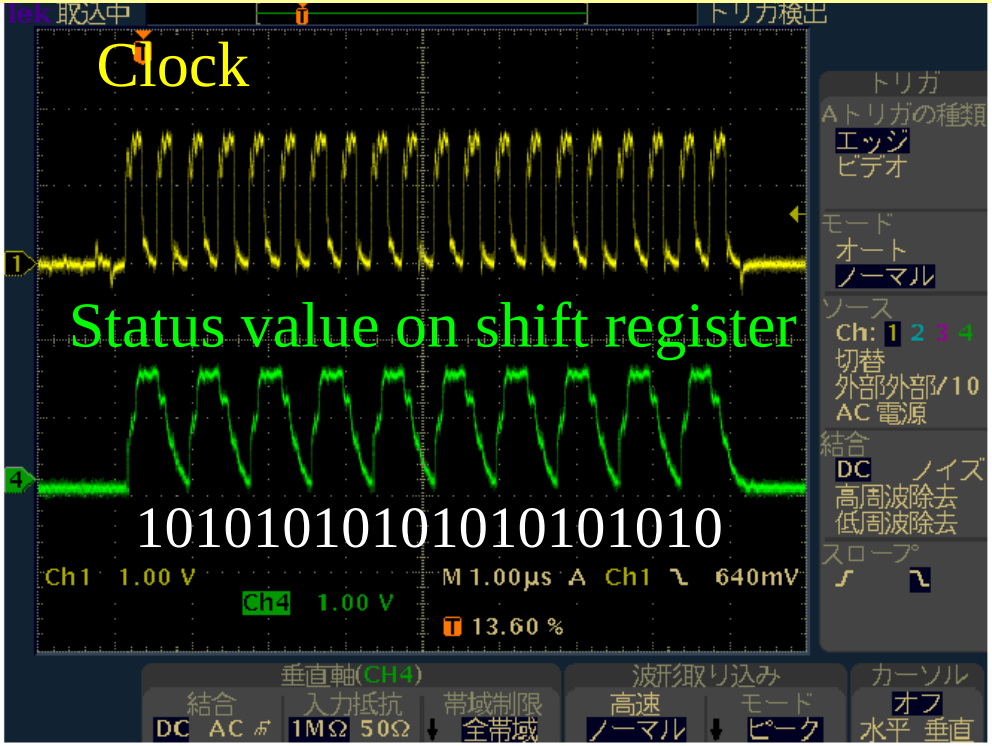
Test board for 2nd prototype



Parameter setting

The behaviors of the shift registers for setting the parameter (gain, filter, offset) are investigated.

Behavior of the shift register in the case that **“101010...”** is written



The output corresponds with the command.

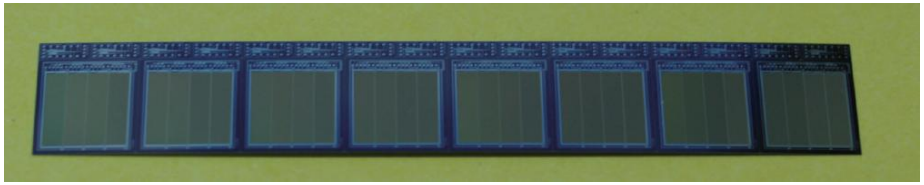
The parameter is set correctly by order of the PC.

Summary and Plan

The 2nd prototype was developed to solve the problems on 1st ASIC.

Second prototype of ASIC

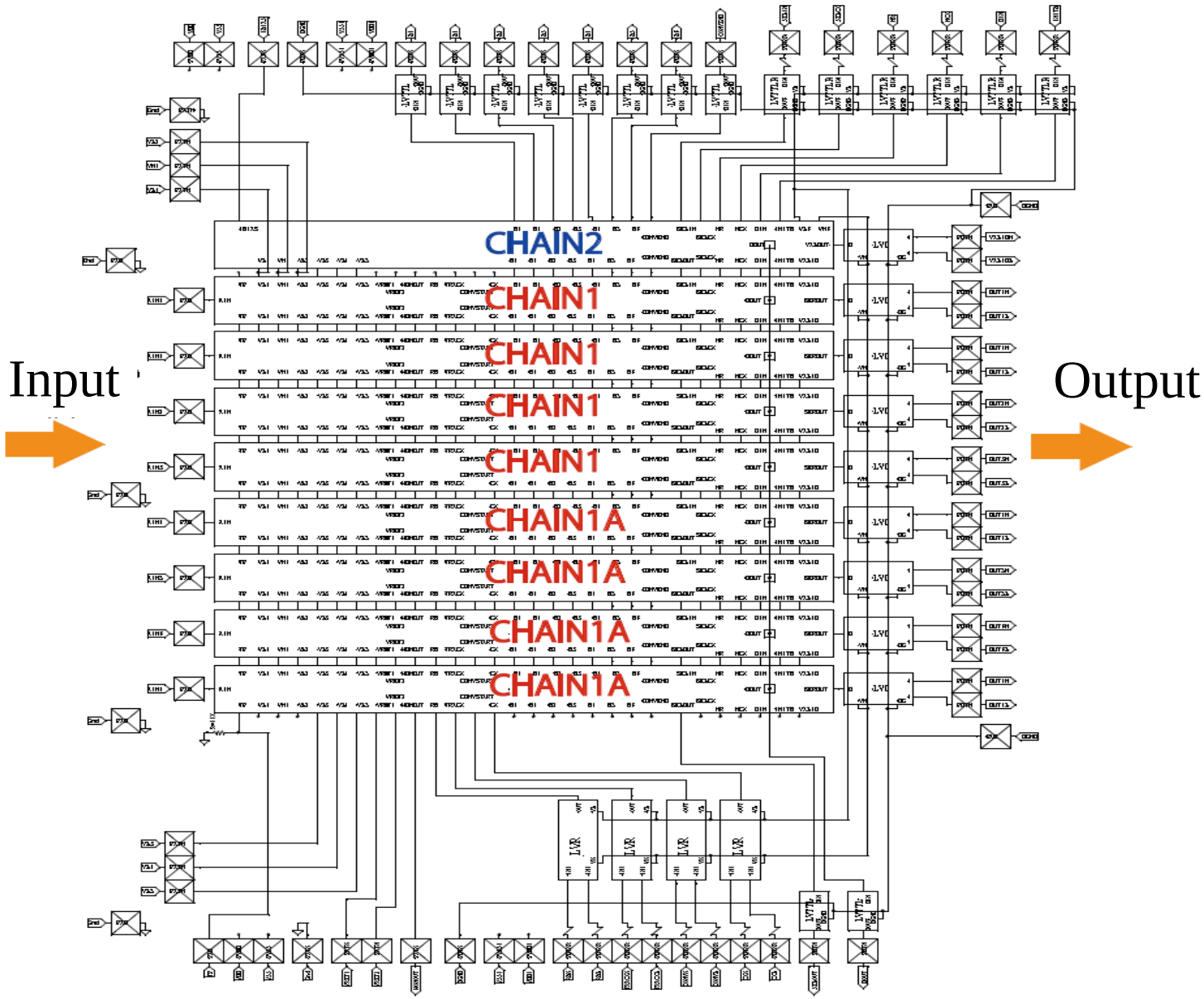
- can be satisfied with the requirements on the readout speed and noise level in the post layout simulation.
- Power consumption [Simulation] : 27 mW/ch
  (requirement: 6 mW/ch)
- We received at the end of Feb. and has been tested the performance.
  - Parameter set → OK
  - **ADC check**.
  - Readout test with **6 μm × 6 μm FPCCD**



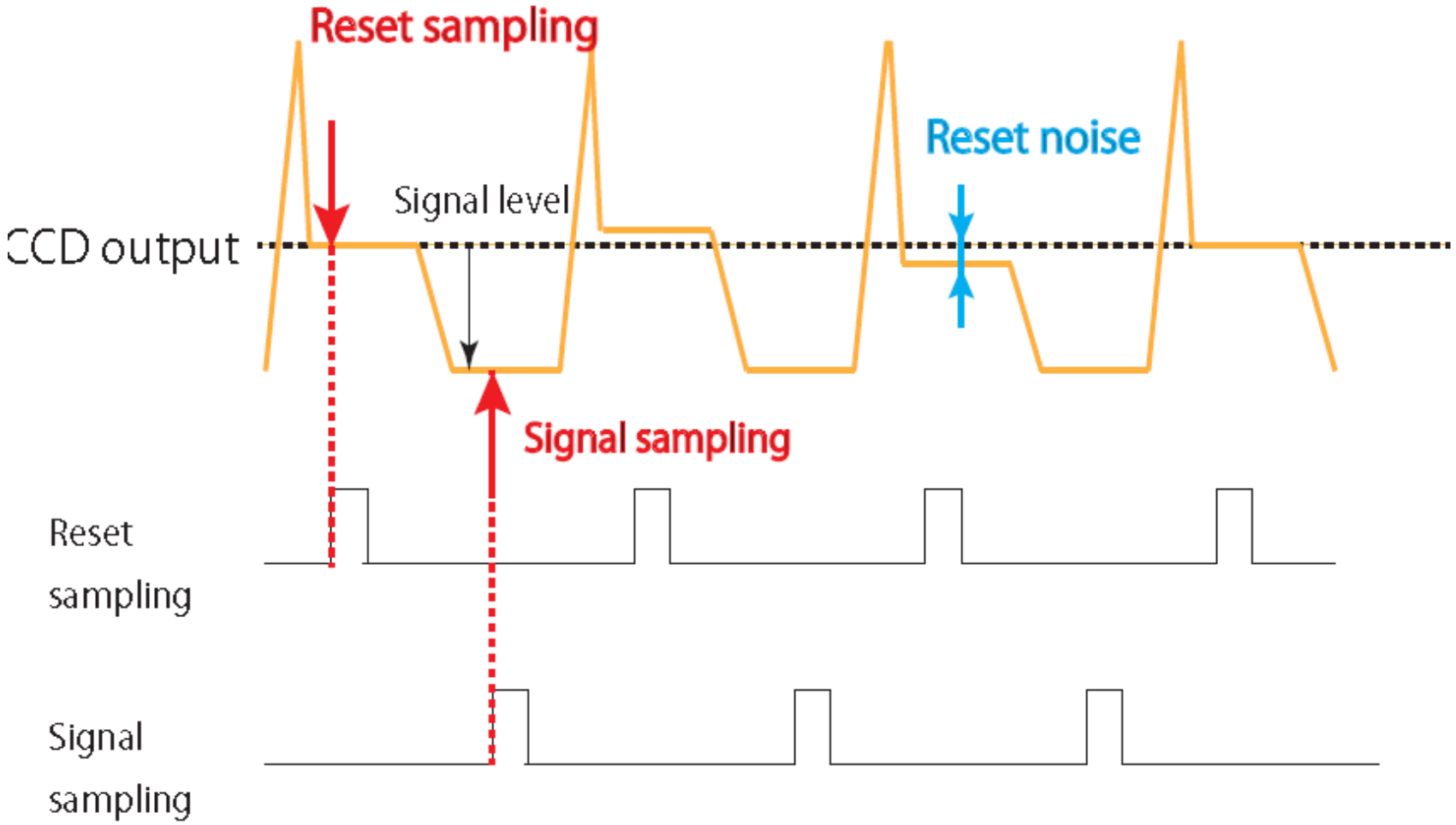
Thickness
50 μm

Back up

ASIC


Input
Output
CHAIN2
CHAIN1
CHAIN1
CHAIN1
CHAIN1
CHAIN1A
CHAIN1A
CHAIN1A
CHAIN1A

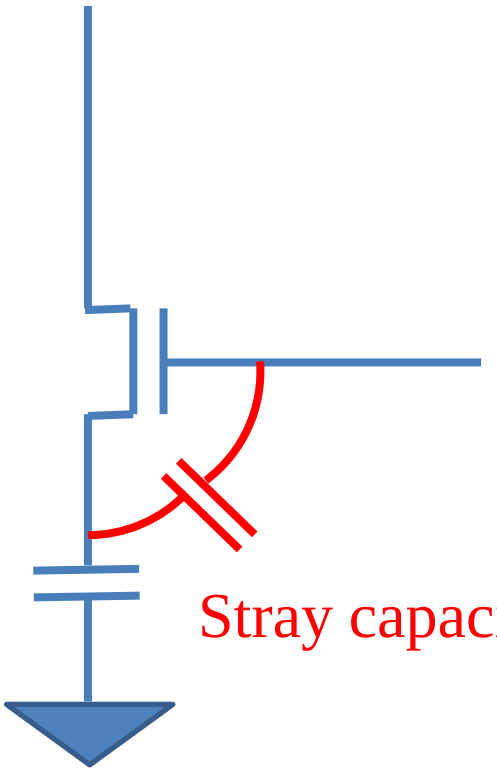
Correlated Double Sampling (CDS)



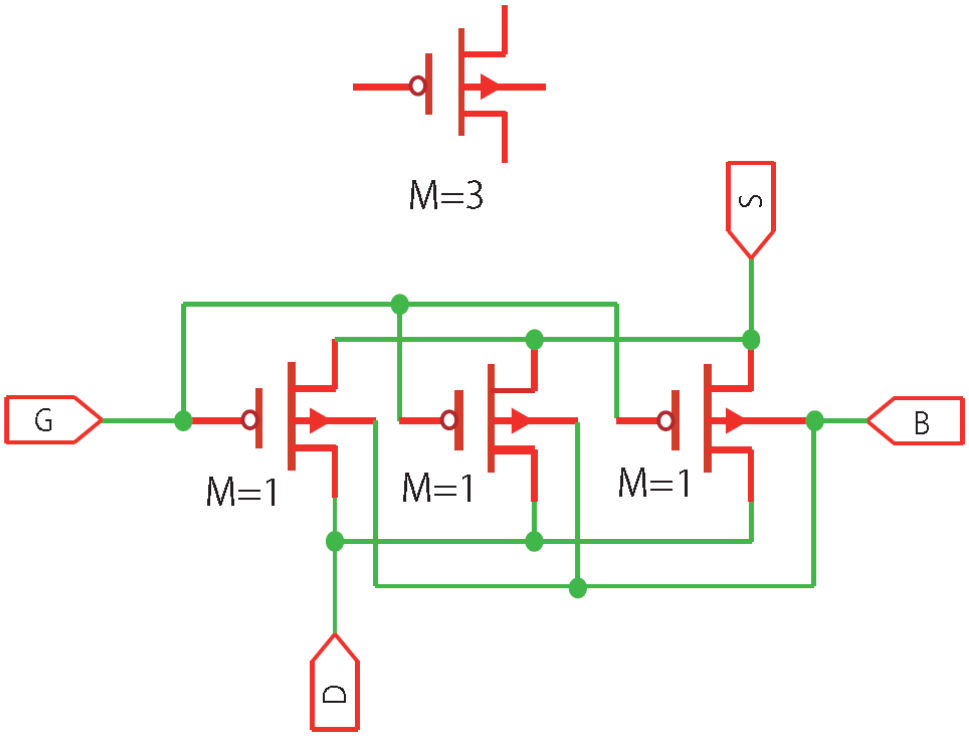
The noise can be suppressed by sampling the difference between the reset and signal level

Measures against stray capacitance in switch

switch



Stray capacitance



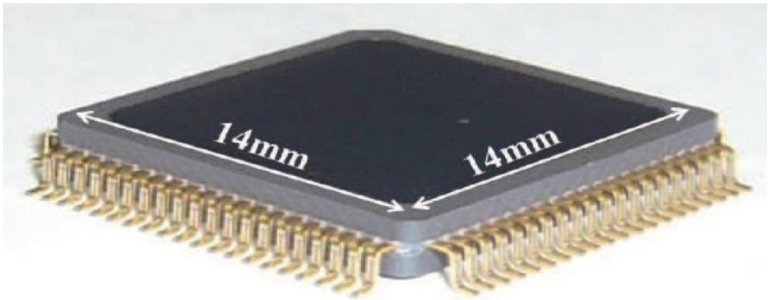
Suppress the effect on the stray capacitance
By tuning the M value which is corresponded
to bit-weighted

1st prototype of ASIC

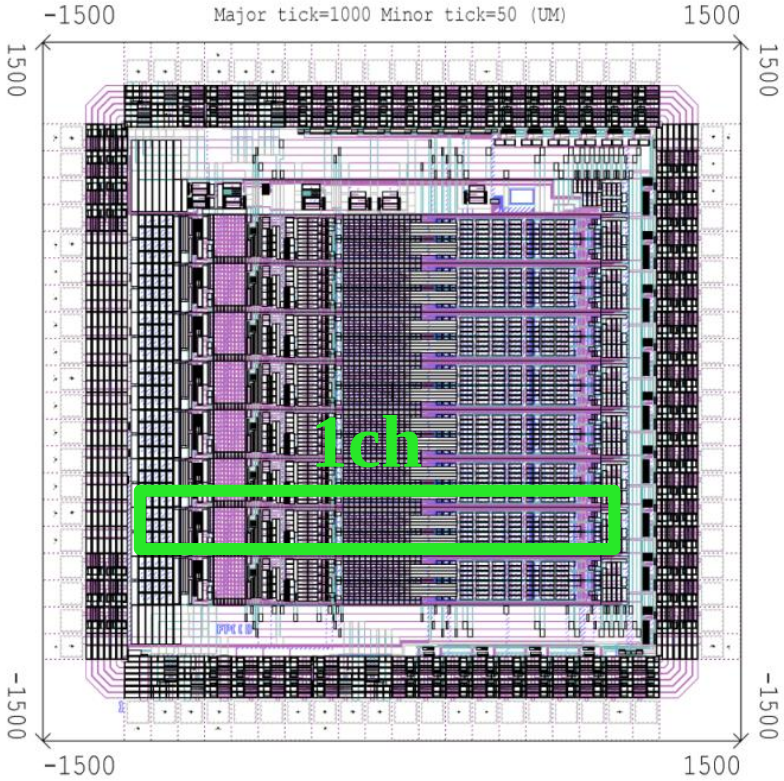
1st prototype ASIC

- Layout by Digian technology
- Produced by TSMC
- Process：0.35μm CMOS
- Number of channel：8
- Size：2.85 mm ×2.85 mm

Packaged ASIC



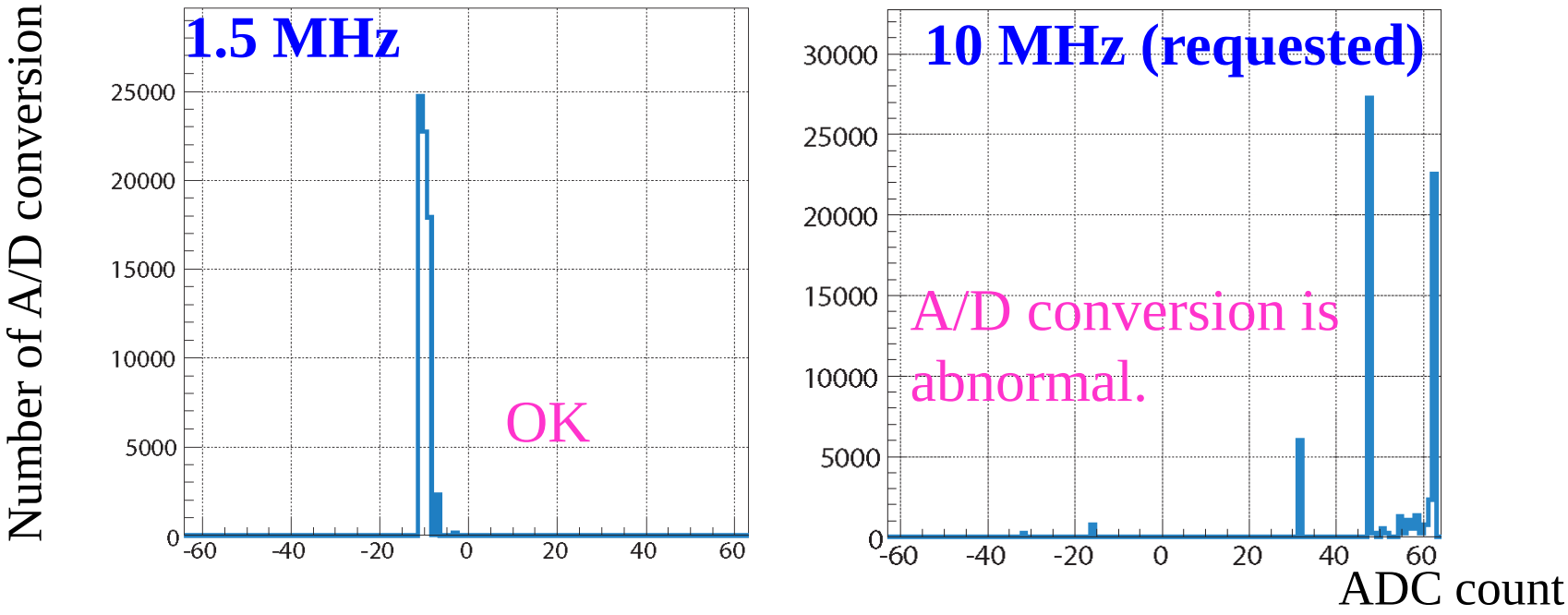
ASIC Layout



Performance check ~Readout speed~

The readout speed was checked by the pedestal distributions

Pedestal distribution (ADC count)



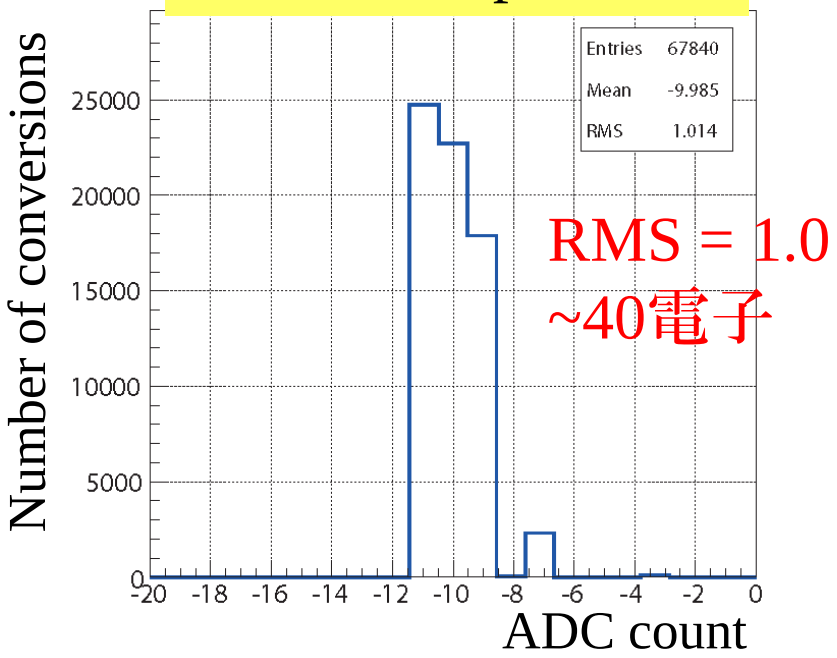
- In case of 10MHz : × → • Short of current to the comparator
  • Stray capacitance
- Upper limit on readout speed ~ 1.5 MHz

From now on, readout speed = 1.5 MHz

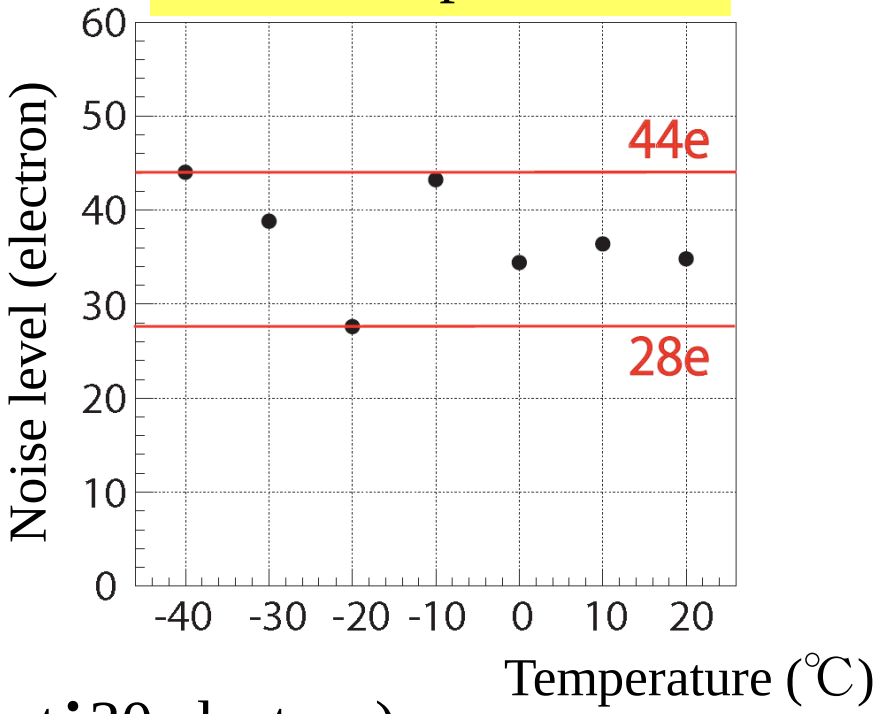
Performance check ~Readout noise~

The readout noise is estimated by the pedestal distribution.

Pedestal distribution at room temperature



Dependence of noise on the temperature



- Noise level = 40 electron (Requirement：30 electron)
  - 1ADC count = 40 electron → Bad resolution to estimate the noise
- Small dependence on temperature (Cryostat : -50℃)

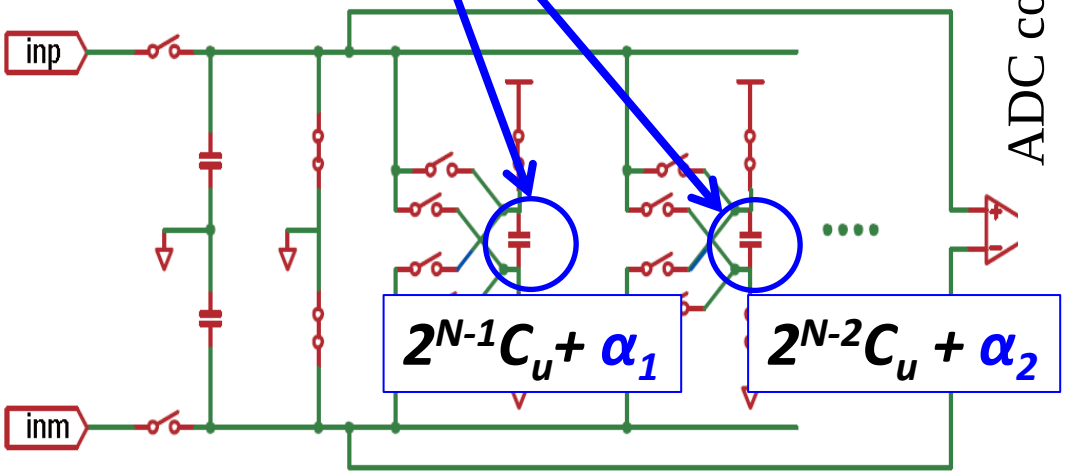
Performance check ~Linearity~

The source of the big jumps on the output was examined by simulation.

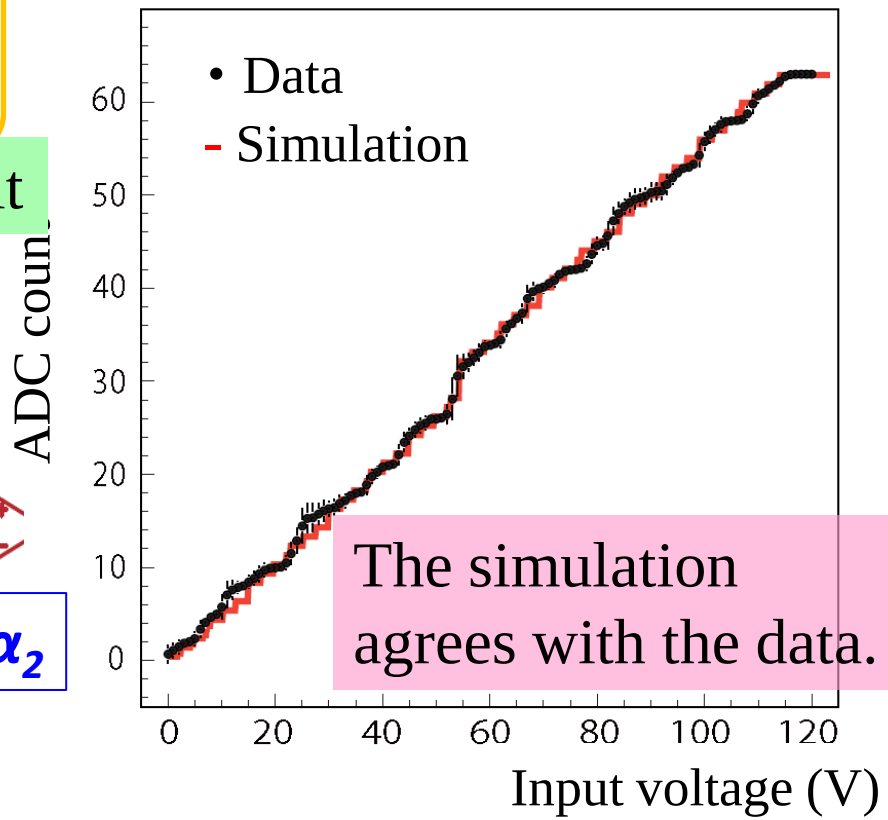
Simulation

The ratio of the capacitance-array in the ADC is changed.

corresponding to bit



ADC count and input voltage



The simulation agrees with the data.

Source of the big jumps on the output = Stray capacitance in ADC