Development of readout ASIC for FPCCD vertex detector

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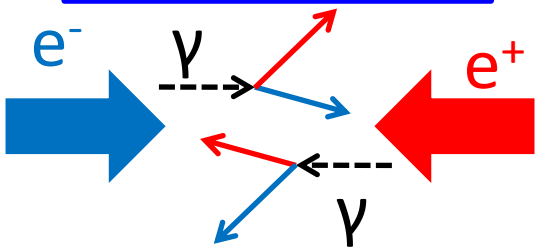
FPCCD vertex detector

■ Pixel occupancy < ~1%

– Large pixel occupancy in the Inner most layer due to pair background events.

➢ Fine Pixel

Pair background



■ Fine Pixel CCD(FPCCD)

– geometry: 3 double layers

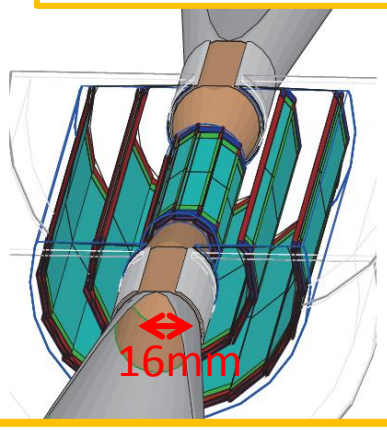
- Pixel size: **5 ×5 um^2**
- Sensitive region: 15 um (full depleted)

– 20,000 × 128 pix/ch

– total #ch ～6,000ch

– **Total ~10^{10} pixels**

Vertex detector



Thickness 50um FPCCD sensor

FPCCD vertex detector

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➢ Fine Pixel

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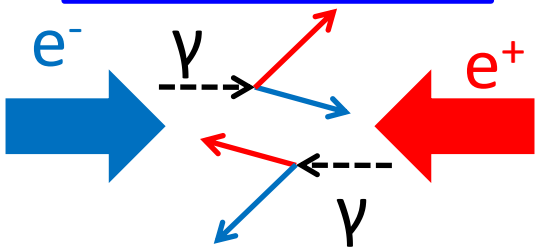

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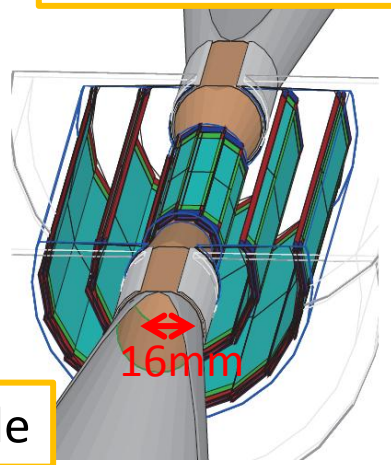
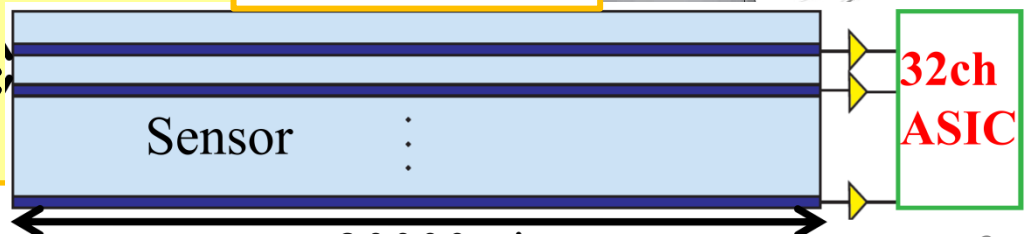
Vertex detector

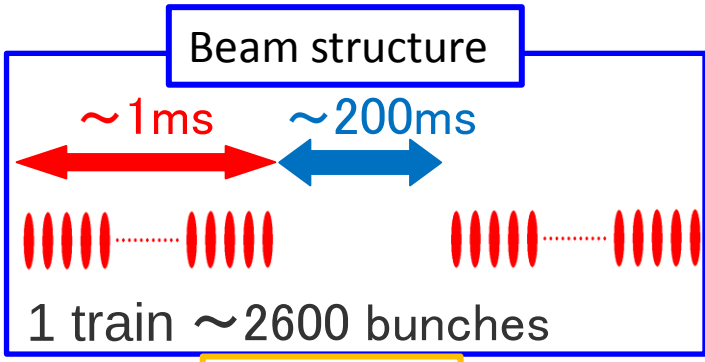


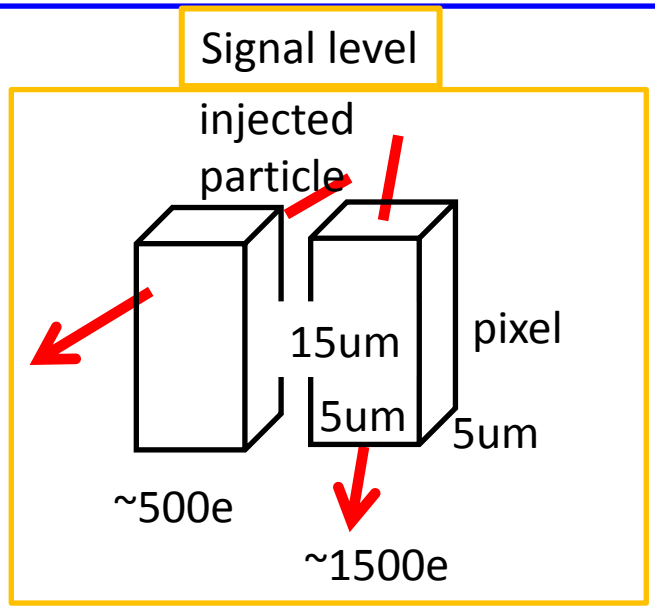
Sensor module



Requirements to readout system

- Readout speed > 10Mpix/sec
  - Readout in inter-train time(200ms)
  - 20,000x128pix/200ms
- Noise level < 30e-
  - Small signal : ~500e-
- Power consumption < 6mW/ch
  - Placed in -50℃ cryostat
  - Total power consumption<100W





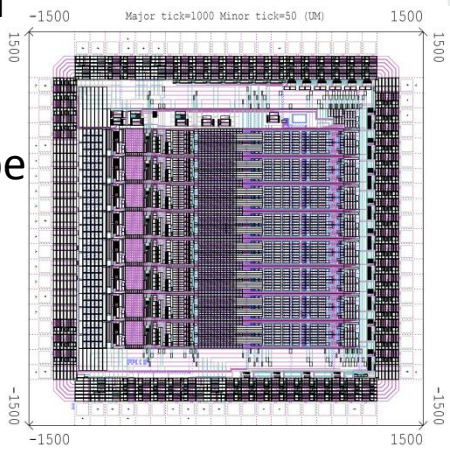
➢ Develop readout system that meets these requirements

Prototype of readout ASIC

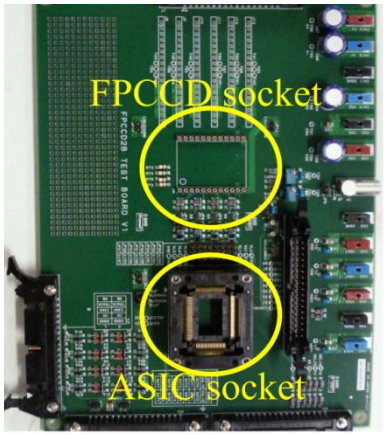
- Aim of prototype
  - readout speed>10Mpix/sec
  - Noise level < 30e-
  - Power consumption<6mW/ch

1st/2nd 3rd prototype

Layout 2nd prototype of readout ASIC



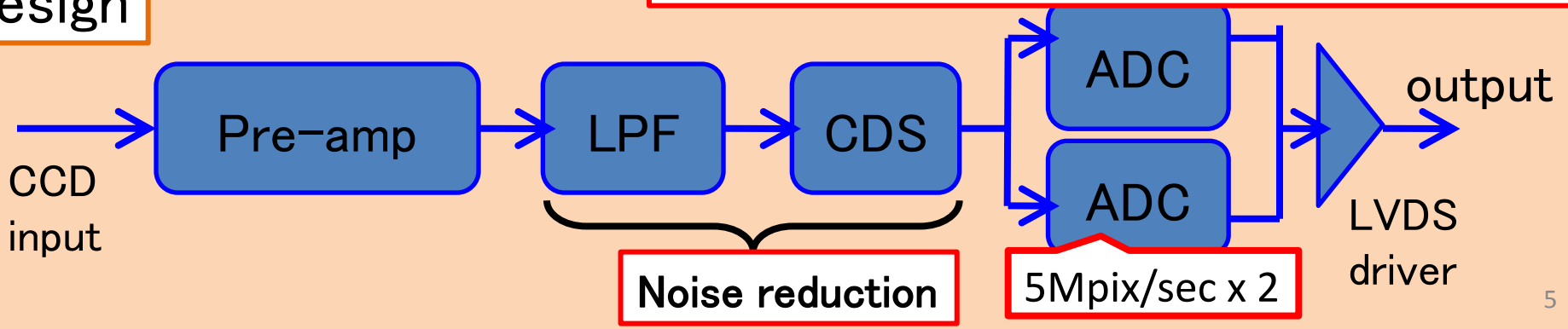
Test board 2nd prototype ASIC



- 2nd prototype of readout ASIC
  - 0.35umTSMC process
  - # of channels : 8 ch
  - Chip size : 4.3mm × 4.3mm
  - 8 bit signal(100MHz CK)

Charge sharing ADC
(low power consumption & relatively highspeed)

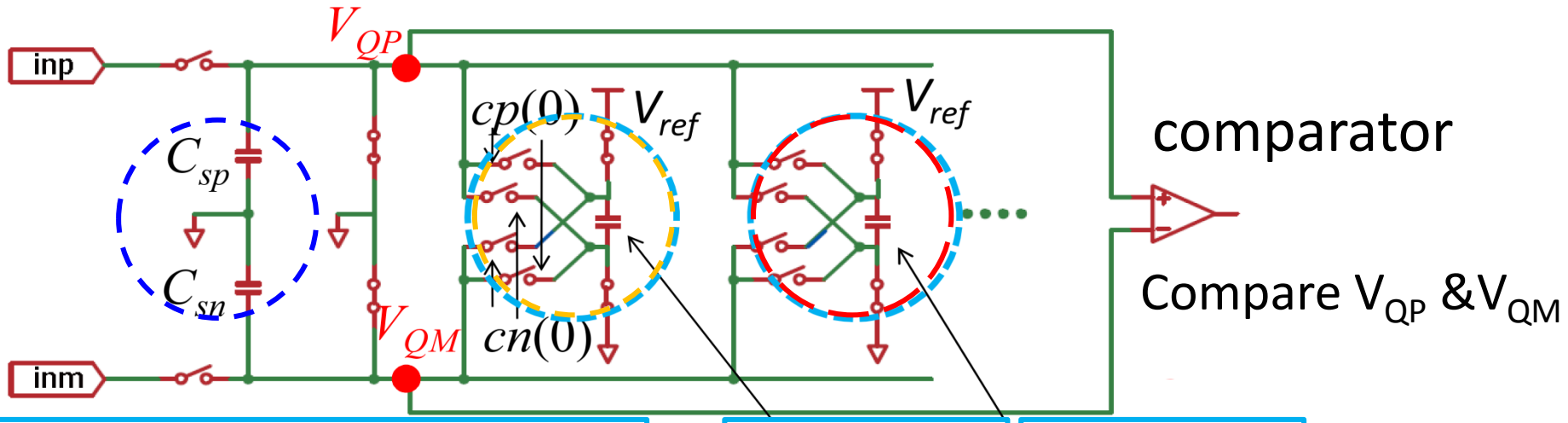
design



Charge sharing ADC

- mechanism

1. store signal at C_{SP} and C_{SN} and compare V_{QP} and V_{QM}.
   →determine most significant bit (MSB)
2. switch on either cp or cn, depending on result 1.
   →compare V_{QP} and V_{QM} →determine second bit
3. … and so on..



Capacitance corresponding to bit weight

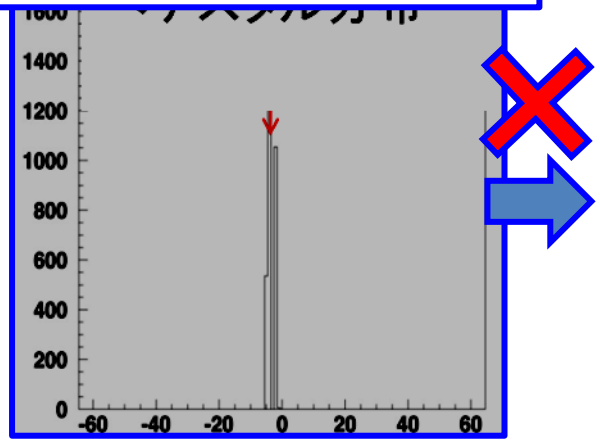
2^{N-1}Cu: 2^{nd} bit

2^{N-2}Cu: 3^{rd} bit

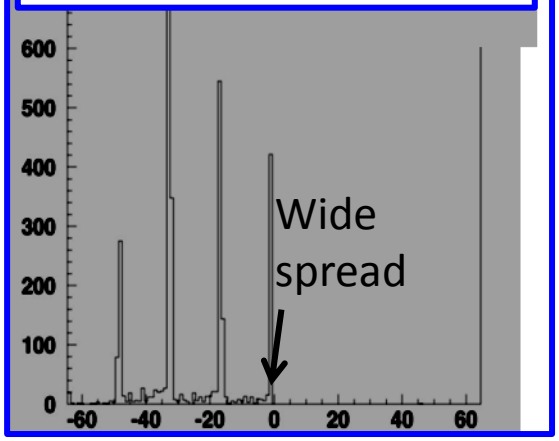
Problems of 1st prototype

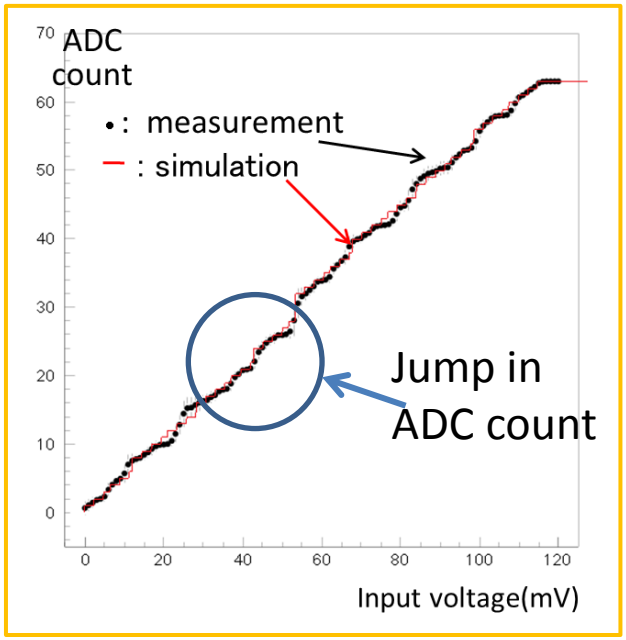
- Limitation of Readout speed (1.5Mpix/sec)
  - Possibility of current shortage to ADC comparator.
- Large jumps in ADC output
  - As an effect of stay capacitance, there is a possibility that capacitor ratio isn't corresponding to bit weight.

1.5Mpix/sec ADC output
Pedestal distribution



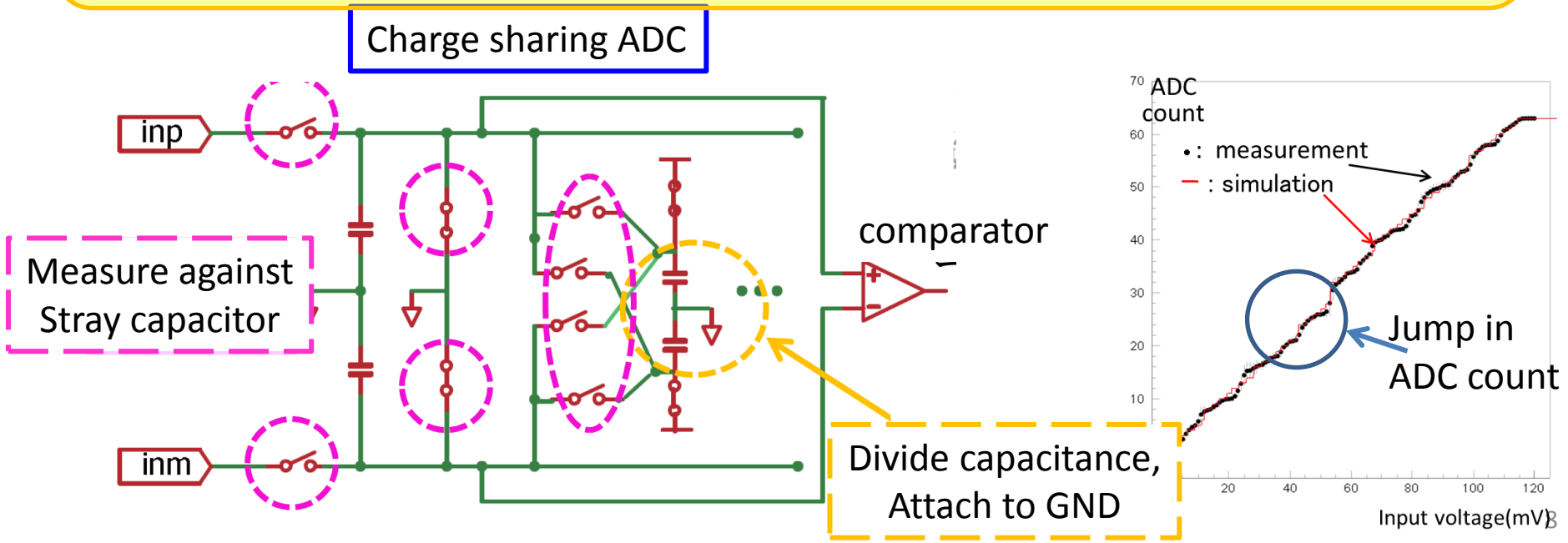
5Mpix/sec ADC output
Pedestal distribution





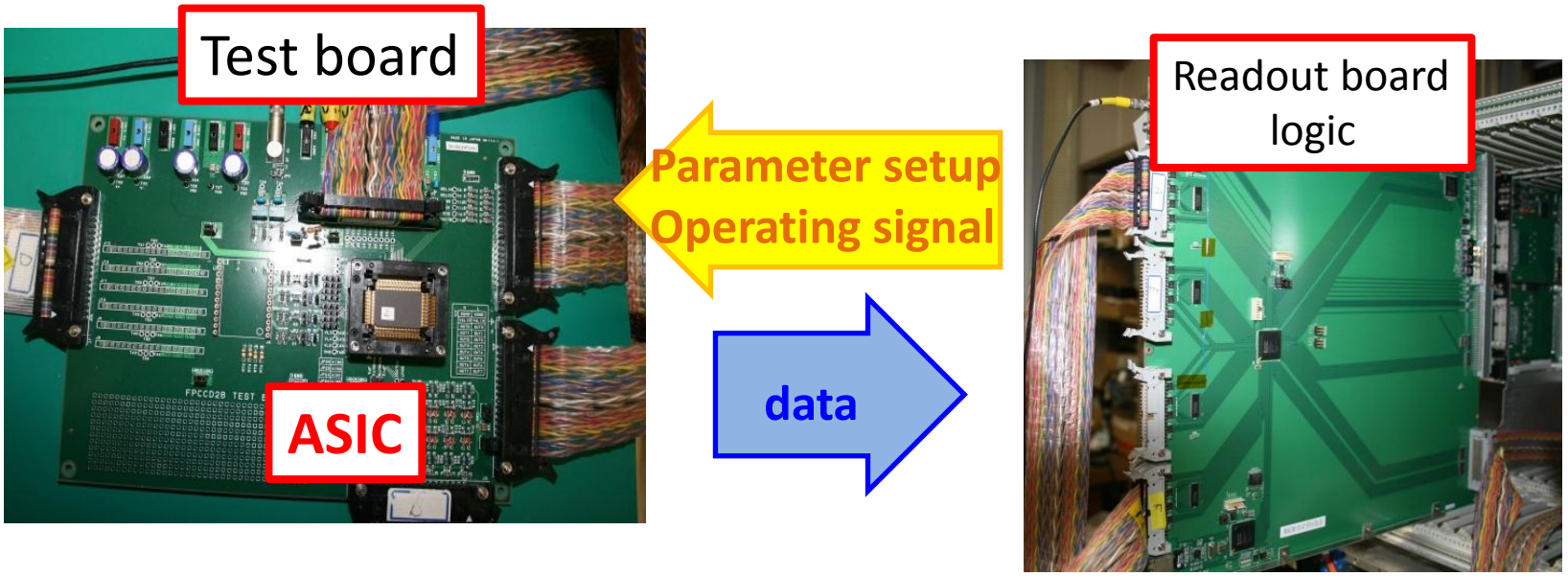
Changes in 2nd prototype

- Countermeasure against readout speed limitation:
  - Increase current supply to ADC comparator by increasing # of pins 80→100
- Countermeasure against jumps in ADC count:
  - Suppress the effect of stray capacitance attached to switches and in between GND.



Setup for 2nd prototype testing

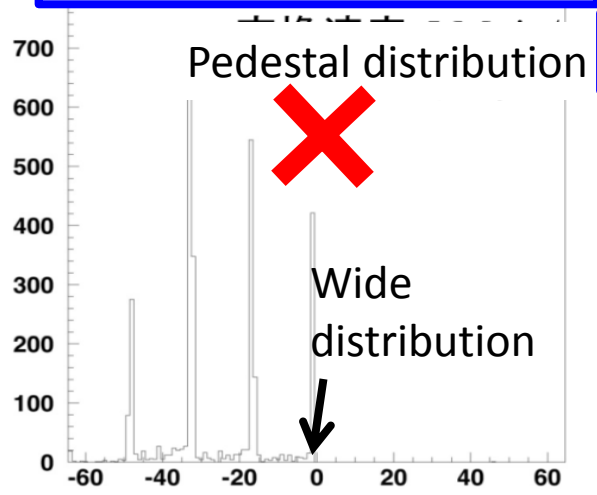
- Implement logic circuit in FPGA.
- Data transfer via VME bus.
- SiTCP usable as well.



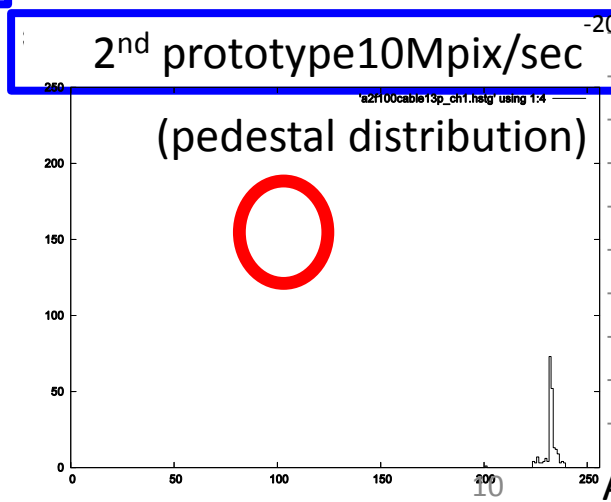
Readout speed of 2nd prototype

- **Verified 10Mpix/sec(100MHz CK) operation**
  - Currently evaluating of linearity (Residual distribution)

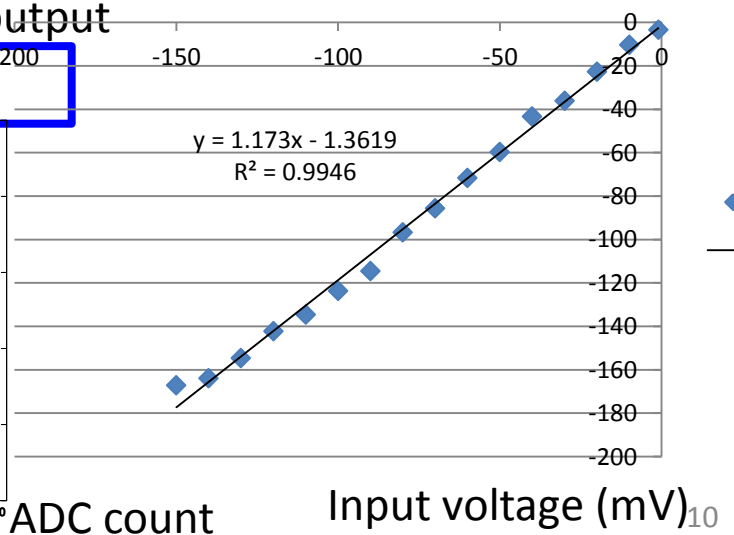
1st prototype 5Mpix/sec



2nd prototype10Mpix/sec



2nd prototype
10Mpix/sec linearity



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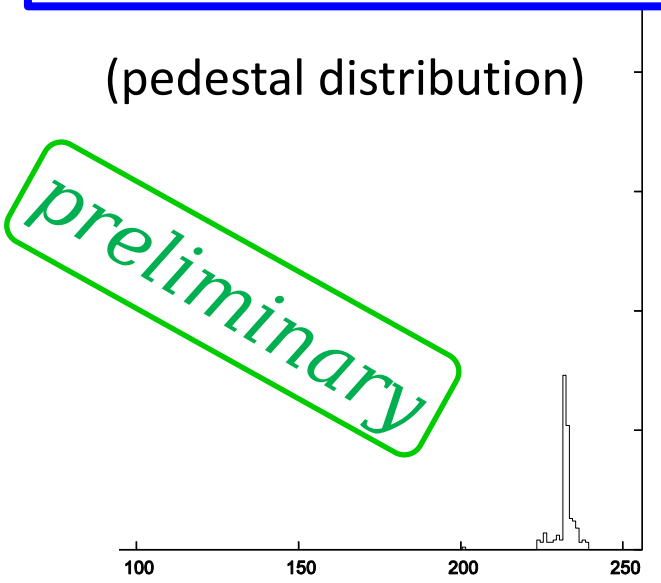
noise level of 2nd prototype

- Required noise level<30e-
  - Measured noise level ~**41e-**
    - ➢currently evaluating noise features (Gain ,LPF dependence etc..)

2nd prototype10Mpix/sec

(pedestal distribution)



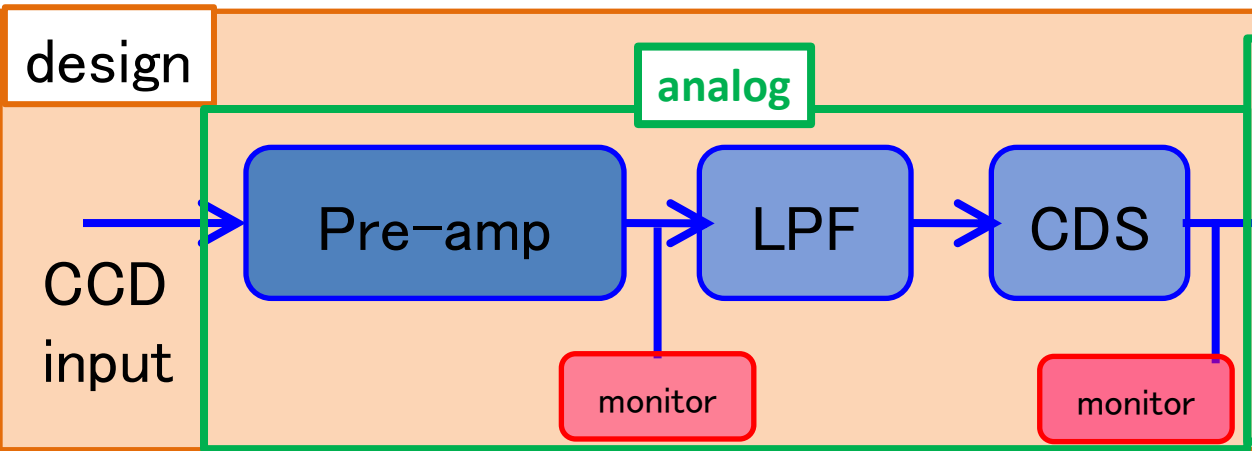
Pedestal to noise(electron) conversion

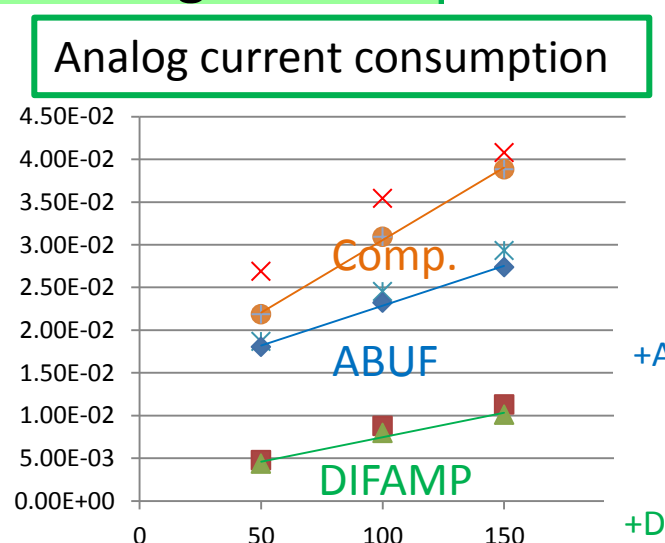
$$1\text{ADC} \sim \text{gradient} \times \frac{1(pF)}{20(pF)} \times \frac{1(e^-)}{5(\mu V)} \text{ electron}$$

Power consumption counter measurements

- Required power consumption < 6mW/ch
  - Measured power consumption 30.8mW/ch (≒simulation)
  - Digital analog power consumption in compatible order.
  - ➢ Drastic changes needed. Process:0.35um→0.25um(or 0.18um)

- changes in next prototype (analog)
  - enable to turn monitor circuit(analog buffer)off
  - Substitute LPF,CDS with low power consuming ABUF





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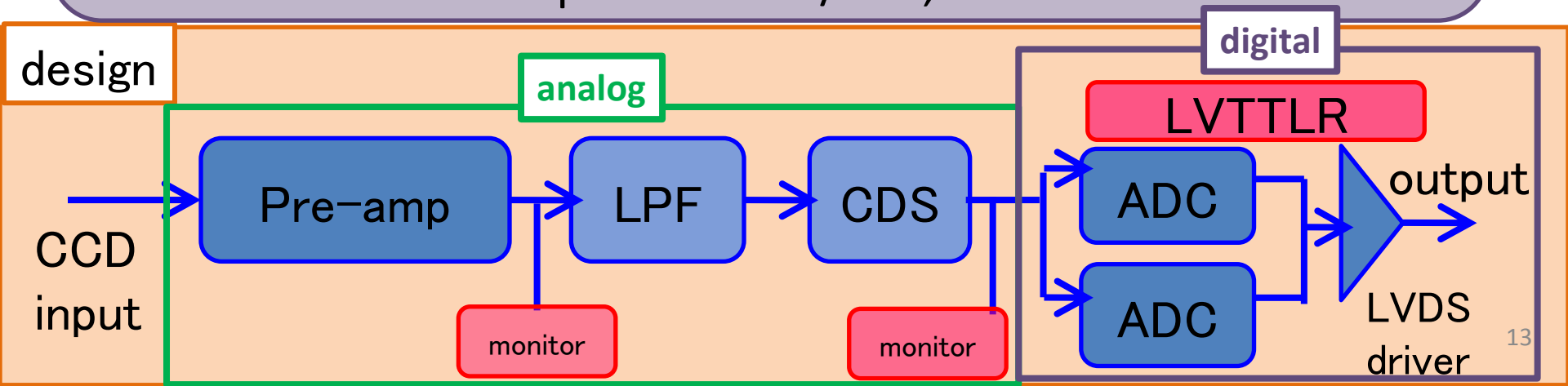
- changes in next prototype (digital)
  - Change so there is no DC current in LVTTLR(receiver for parameter setting signal.
  - current consumption:1.3mA/cell , maximum 22mA



summary

2nd prototype was developed to meet readout speed and noise level

- Readout speed
  - **Succeeded in operating under 10Mpix/sec readout speed , which was difficult in 1st prototype.**
- Noise level : 41e- (preliminary)
- Power consumption
  - Measured power consumption 30.8mW/ch
  - Through simulation , methods to achieve low power consumption are under review.

	Requirement	measurement
Readout speed	10Mpix/sec	10Mpix/sec
noise	30e-	41e-
Power consumption	6mW/ch	30.8mW/ch