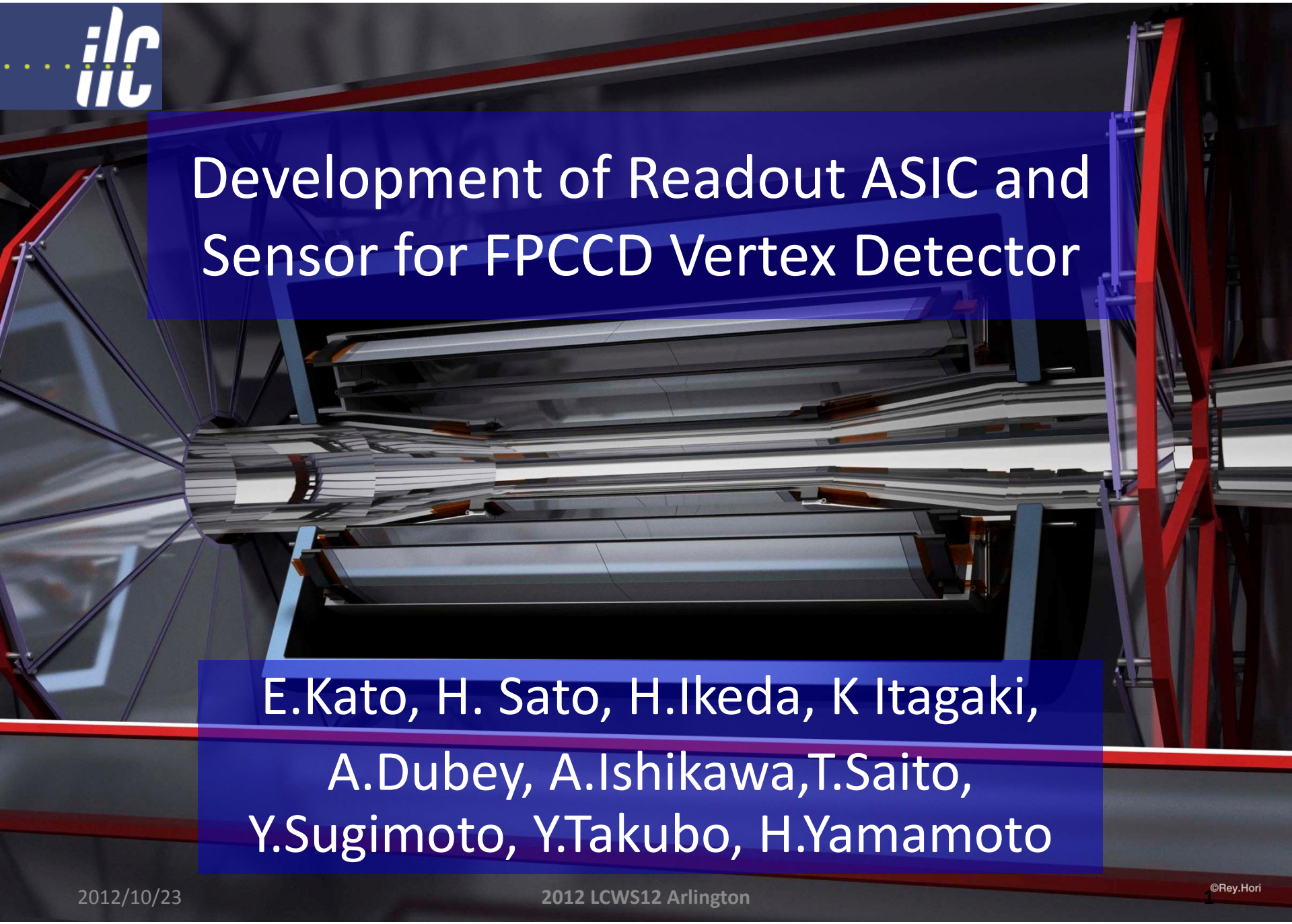

Development of Readout ASIC and Sensor for FPCCD Vertex Detector

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A.Dubey, A.Ishikawa,T.Saito,
Y.Sugimoto, Y.Takubo, H.Yamamoto

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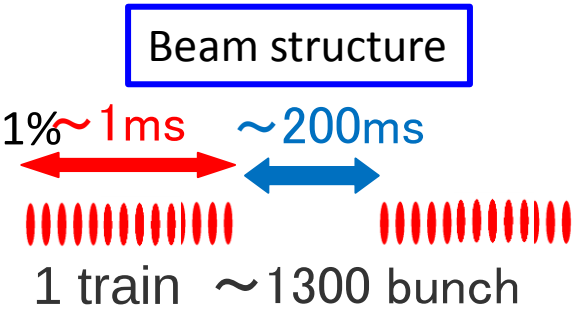
FPCCD features

■ vertex detector
- High impact parameter resolution → near IP
- Accurate tracking → pixel occupancy~1%



➢ Finely segmented pixel

■ FPCCD(FinePixelCCD)vertex detector

pixel size 5×5μm² → ☺ high position resolution; ☹ faint signal

thickness, epi :15μm, Si 50μm → ☺ low multiple coulomb scattering

fully depleted → ☺ high 2 track separation

3 doublet geometry → ☺ BG resilient

inter train readout → ☺ no beam induced RF noise

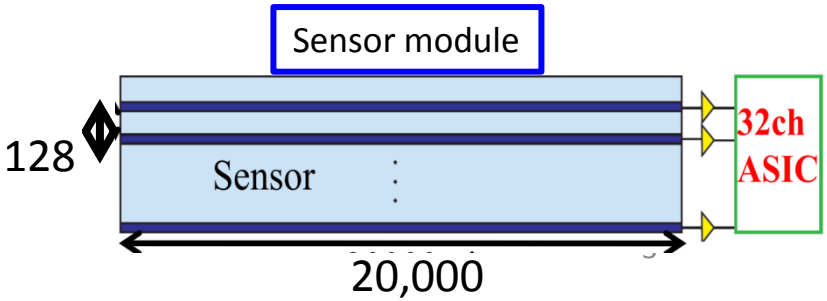
total # pix : 1.6×10¹⁰ → ☹ high speed readout

TOPIC

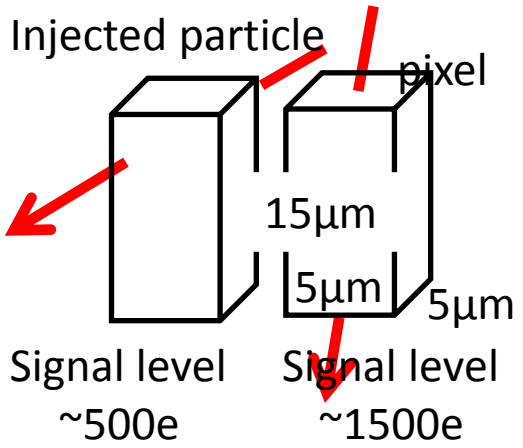
➢ Develop Readout ASIC & CCD for FPCCD

Requirements for CCD and readout ASIC

- readout speed> 10Mpix/sec
  - Readout all pixels within Inter train time(200ms)



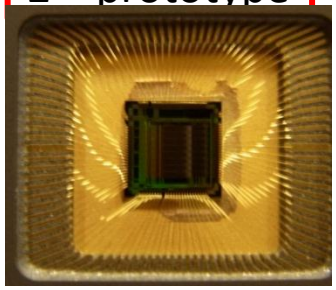
- signal meas. accuracy < 50 e-
  - Faint signal level : ~500 e-
  - Noise + AD conversion accuracy< 50 e-
- power consumption < 6mW/ch (ASIC)
  < 10mW/ch (CCD)
  - Placed in -40℃ cryostat(-40℃)
  - Total power consumption <100W



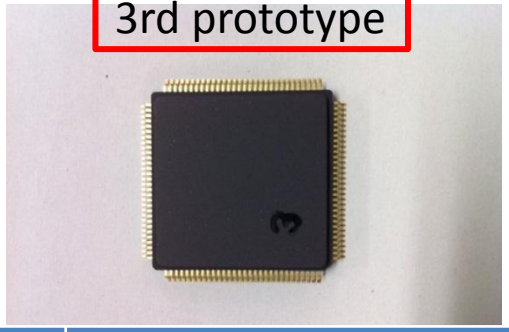
➢ Develop readout ASIC & CCD that satisfies all requirements

ASIC Prototype

2nd prototype

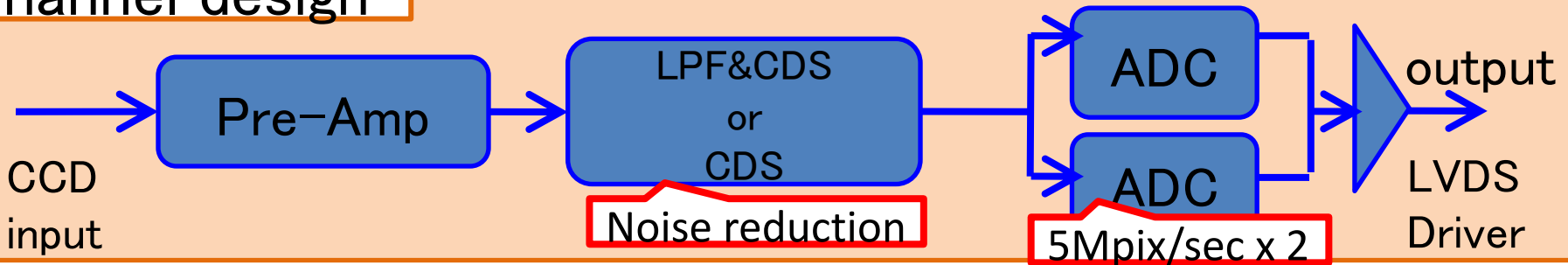


3rd prototype



Chip parameters	2nd prototype	3rd prototype
process	0.35um	0.25um
Chip area	4.3x4.3mm2	3.7x3.75mm2
Gain coverage(from CCD)	12.5~200 (8 steps)	32~64(2 steps)
# of channels	8ch	8ch
Input capacitance form CCD	20pF	3.2pF

Channel design



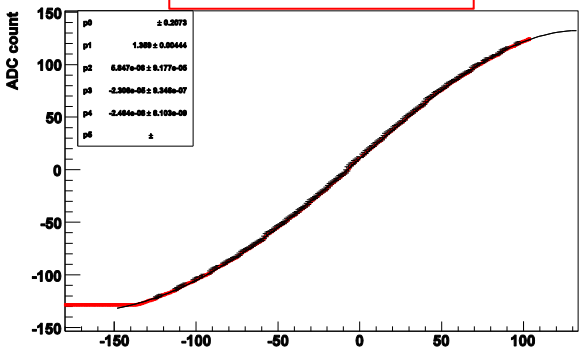
ASIC features & improvements1

- Power consumption
  - Meas. 30.6 mW/ch →simulation4.8mW/ch (peak 5.4mW/ch)

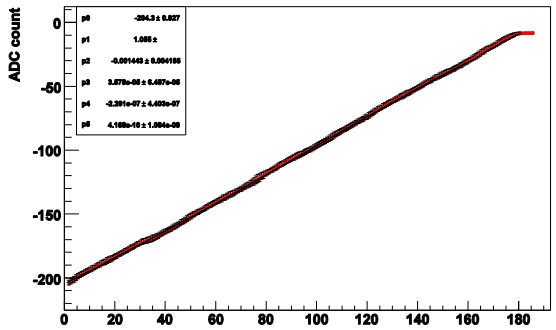
- INL(integral non linearity)
  - Shows curvature in linearity. Caused upstream circuits.

INL 17% → < 2%

2nd prototype



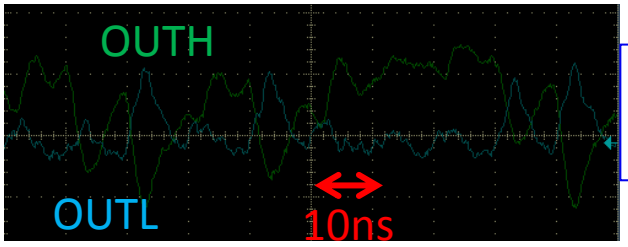
3rd prototype



ASIC features & improvements2

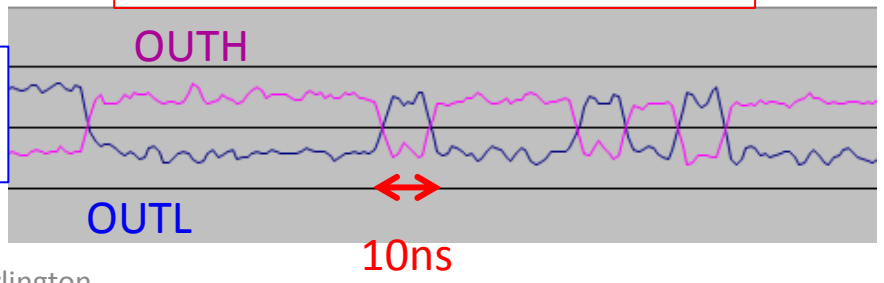
- Radiation tolerance
  - 3rd prototype implemented DICE FF: radiation hardened by design flip-flop with high single event effect(SEE) immunity.
- baseband transmission
  - 10Mpix/s = 100MHz ADC comparator CK
  - Return zero→non return zero
  - Longer high period(10ns), Easy sampling

2nd prototype: return zero



Measured LVDS output signal

3rd prototype: non return zero

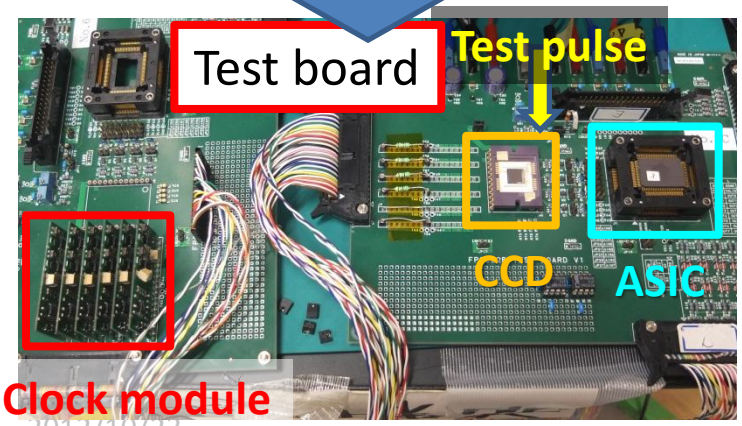


Setup

VME based old system

readout board

Test board



SEABAS2 based system
1GbE
Compact for beam test
Short cables + FFC higher Reliability@100MHz

SEABAS2 based new system

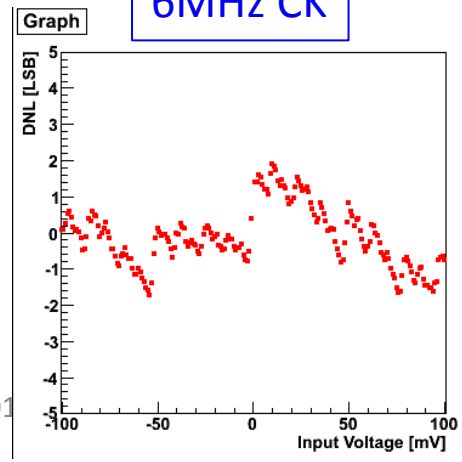
readout board

Test board

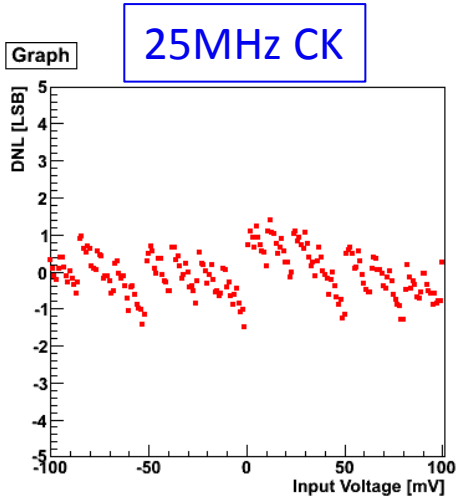
2nd prototype ASIC Frequency dependence

- DNL@low frequency
  - DNL ±1LSB
  - MSB,2MSB displacement from bit weight
- DNL @high frequency (100MHz CK)
  - DNL ±3LSB
  - Due to displacement from bit weight, becomes meta-stable @ bit change. Thus causes bit jump @high freq.
    - ➢ Process change + Speed control @3rd prototype

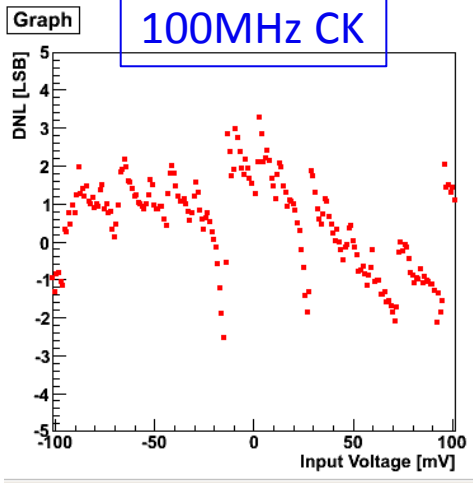
6MHz CK



25MHz CK



100MHz CK



Measurement accuracy

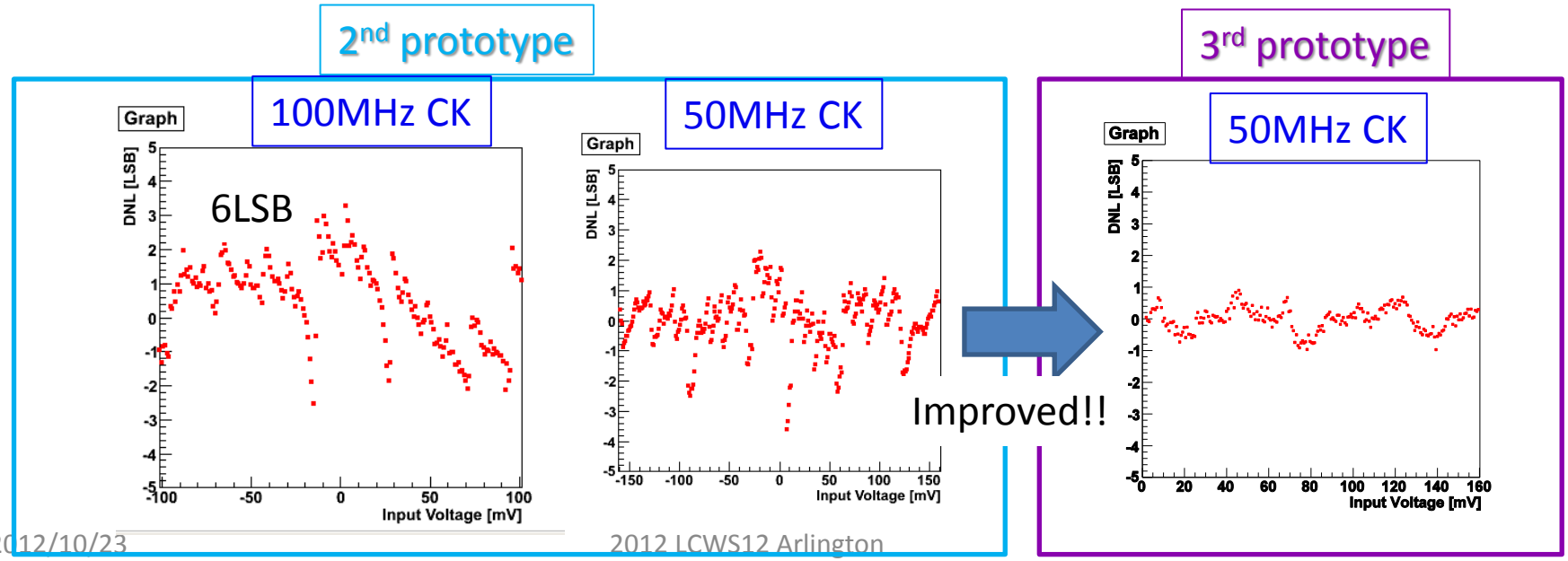
■ $meas.accuracy = \sqrt{DNL^2 + pedestal^2}$

<For 2nd prototype> (input capacitance=20pF)

$meas.accuracy$ = ~16 e- **＜30 e- required**

<For 3rd prototype> (input capacitance=3.2pF)

$meas.accuracy$ = ~12 e- **＜30 e- required**



CCD prototype

- FPCCD sensor prototype

  Hamamatsu Photonics 2phase transfer CCD

<Pixel size : 12umx12um>

  - Chip size: 8.2mm(H)x7.5mm(V)
  - thickness : epi layer 15um, Si total 50um
  - # of channels : 4 ch

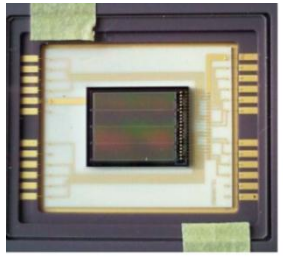
➢ Tested!!

< Pixel size : 6umx6um>

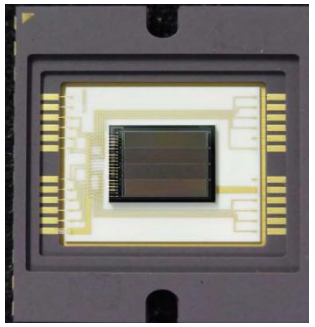
  - Horizontal shift register size 6umx12um
  - thickness : epi layer 15um, Si total 50um

➢ Working! Now testing with 3rd prototype ASIC

12um^2 prototype



6um^2 prototype



$12\mu m$ CCD TEST WITH 2ND PROTOTYPE ASIC

Noise evaluation from pedestal distribution

■ dark current:

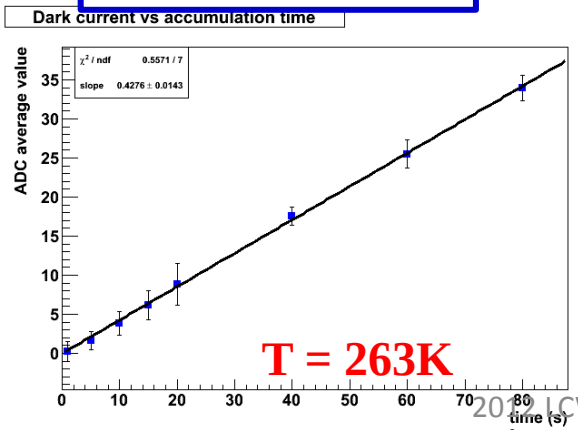
— hot pixel ($Q_{hotpixel} > 5\sigma_{ccd} + \langle Q_{ccd} \rangle$) temporal, temperature dependence well understood

— dark current suppressed under ILC conditions (200ms,-40℃)

■ Pedestal distribution : $\sigma_{(dummy\ pixel)} \fallingdotseq \sigma_{(active\ pixel)}$ @-40℃

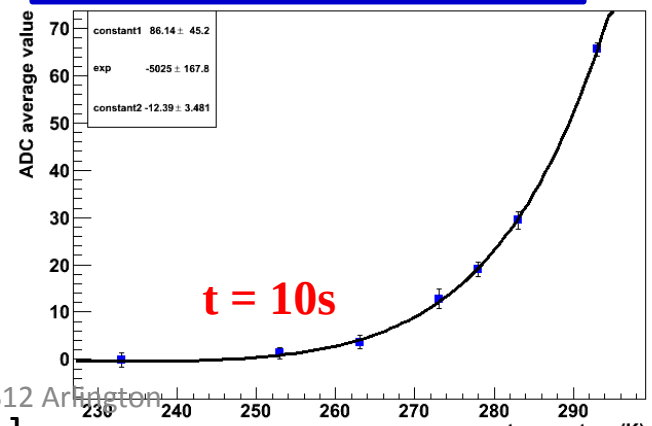
noise: ~55 e-(ASIC indep. test within 16e-)

Time dependence



Time [s]

Temperature dependence

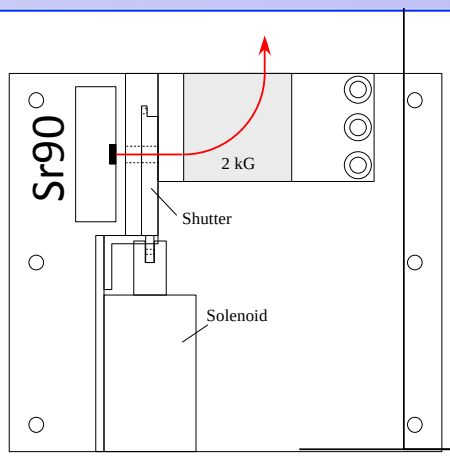


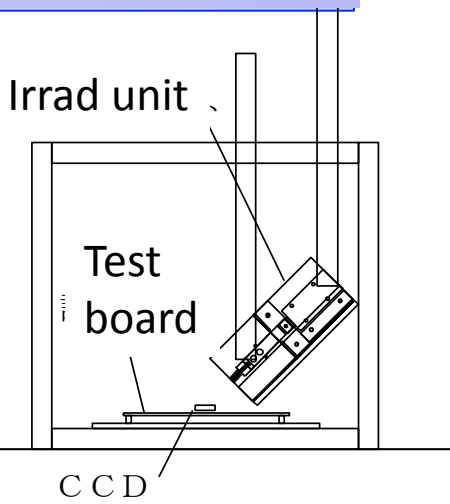
temperature[K]

Sr90 β-ray measurement

■Setup

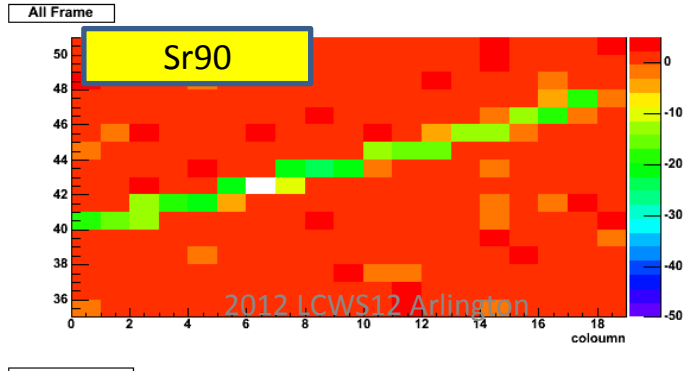
Irrad unit : select 2MeV β-ray





■Sr90(~10℃,2.5Mpix/s)

- Checked charge distribution with 2MeV β-ray
- Few charge leakage to adjacent pixels.

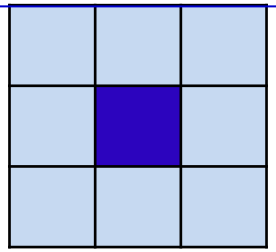


Fe55 X-ray measurement

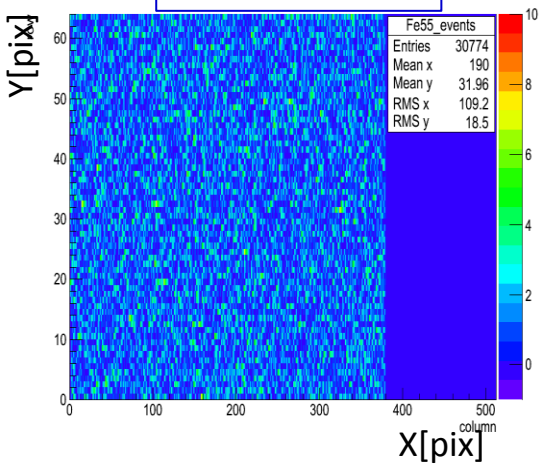
- setup
  - —irrad time10s,-40℃,3000 frames
- S/N：37

  Single pixel hit extraction
- energy resolution: 120 eV

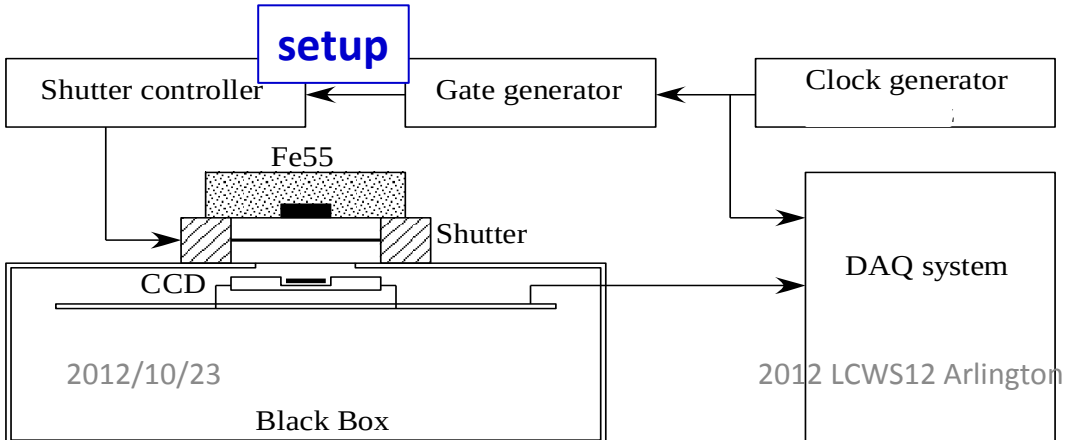
Single pixel hit



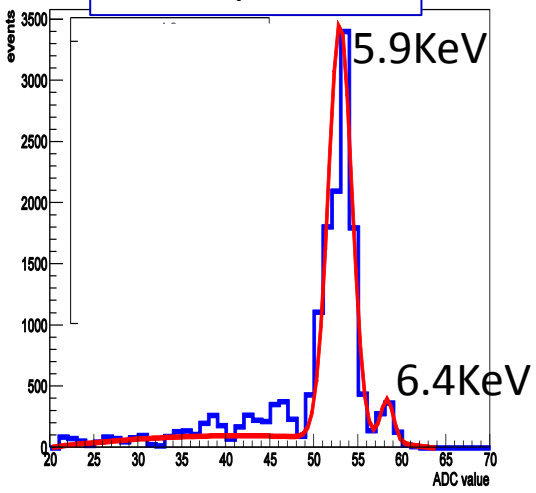
Fe55 hitmap



➢ Highly sensitive, low noise detector!



Fe55 spectrum



CTI measurement with Fe55

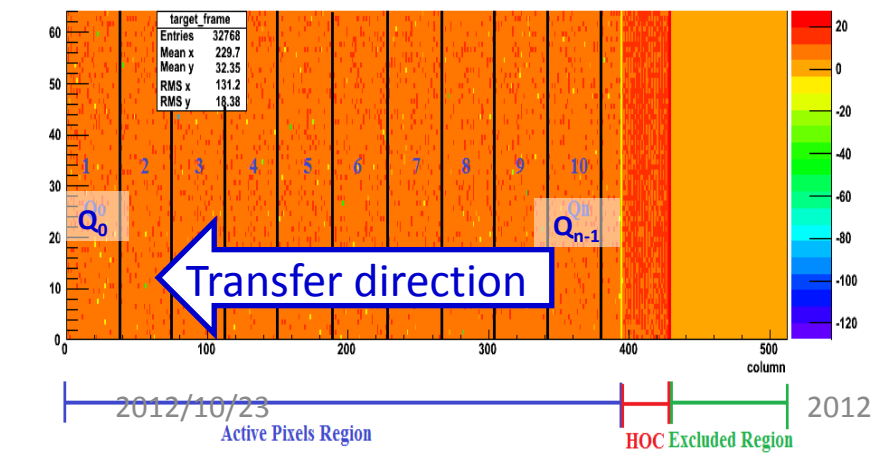
- CTI(Charge Transfer Inefficiency)
  - For high sensitivity, we need high transfer rate(CTE)

  (CTI is degraded by radiation damage)

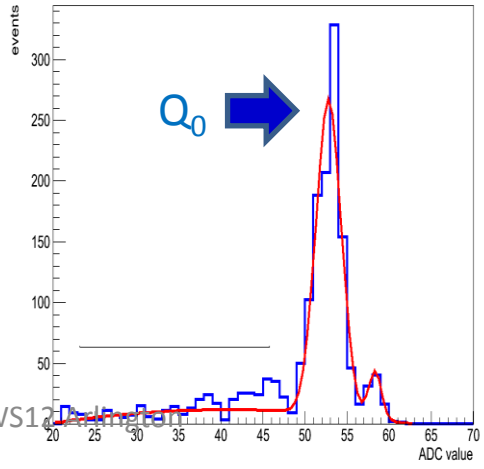
  - $CTI \equiv -\frac{1}{Q_o}\frac{dQ_n}{dn_x}$

Q_n : $meas.signal\ level@\ different\ regions$
Q_0: signal level @closest region
CTI : charge loss per transfer
$Q_n = Q_o - CTI * n_x$

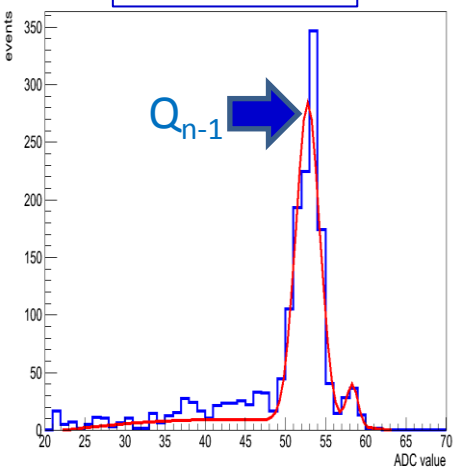
Section when evaluating horizontal transfer CTI



Section 1



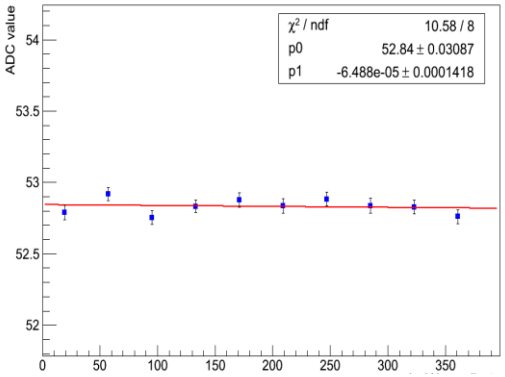
Section 10



CTI meas. results with Fe55

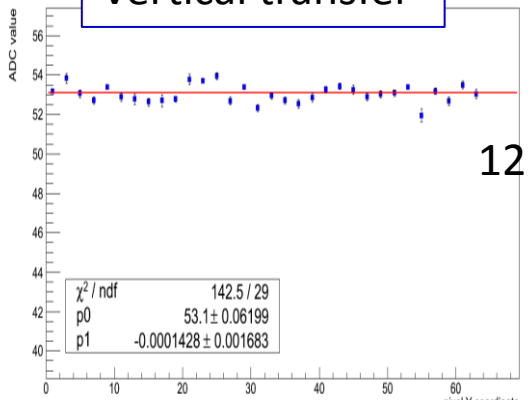
- transfer efficiency
  - No significant inefficiency was seen
  - Transfer rate of most extreme pixel within 1ch ILC sensor module is 97.9 % (largest number of pixels)

Horizontal transfer

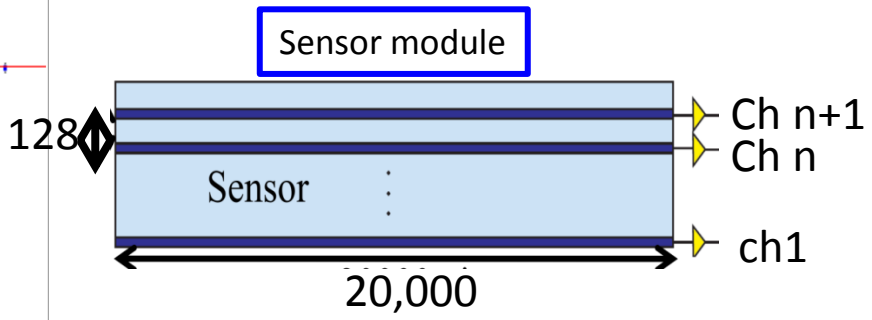


X coordinate

Vertical transfer



Y coordinate



Direction	CTI (per transfer)	Total CTE (%)	
Horizontal	(1.2±2.7)x10^{-6}	98.0±6.0	20,000transfer
Vertical	(0.3±3.1)x10^{-5}	99.9±0.4	128transfer

Transfer efficiency @ most extreme pixel is 97.9 %

Summary & plan

<SUMMARY>

- 3rd prototype ASIC is working!
- 12um CCD + 2nd prototype ASIC
  - Showed promising results
  - S/N, CTI, charge distribution etc
  - ➢ more test will be done with new & improved 3rd ASIC + Finer segmented CCD.

<PLAN>

- 3rd prototype 100MHz CK operation
- 6um CCD + 3rd prototype ASIC
  - Fe55 S/N
- Large wafer + 3rd prototype ASIC
  - CTI measurement