



Performance Evaluation and Software Development of FPCCD Vertex Detector for ILC

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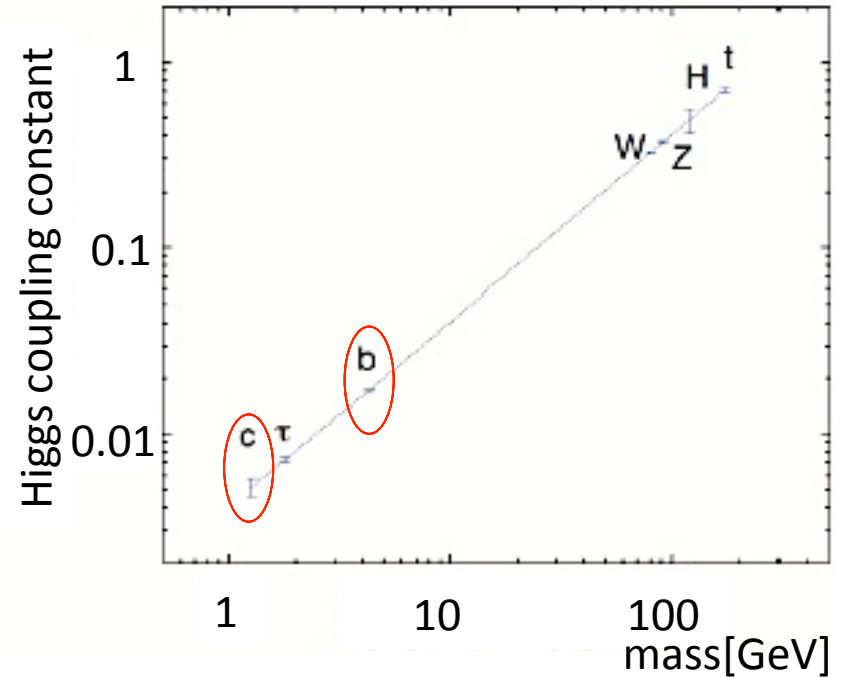
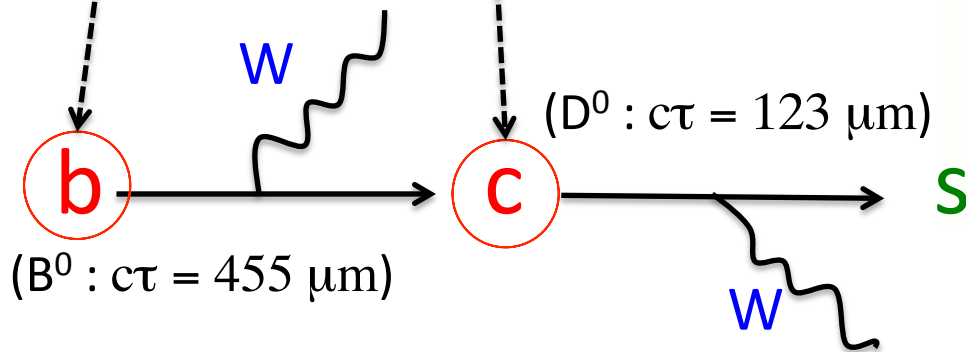
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Road of Vertex Detector

one of the ILC physics goal:
precise measurement of Higgs coupling constant to **c** and **b** (hard at LHC)

precise identification of
 $H \rightarrow bb, cc, gg$ is required



→ We need Vertex detector (VXD) with high performance

Fine Pixel CCD Vertex Detector (FPCCD)

FPCCD's feature: **tiny pixel CCD!**

pixel size : $5 \times 5 \mu\text{m}^2$

sensitive thickness : $15 \mu\text{m}$

total thickness : $50 \mu\text{m}$

~ 10 billion pixels

readout : per 1 train



High IP Resolution!

Low Pixel Occupancy!

But

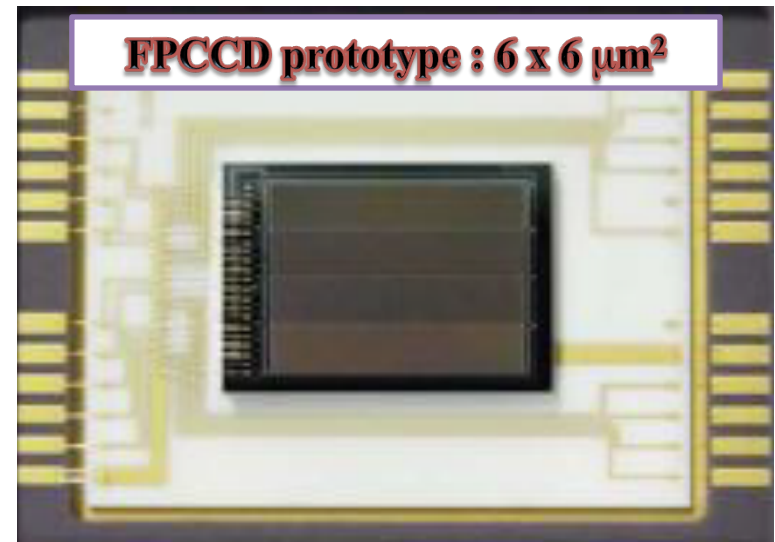
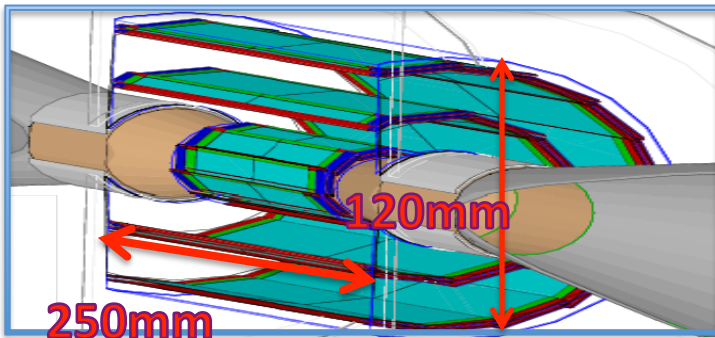
Tracking with many bkg. hits is challenging

1 train (1ms)

rest (199ms)



FPCCD's readout

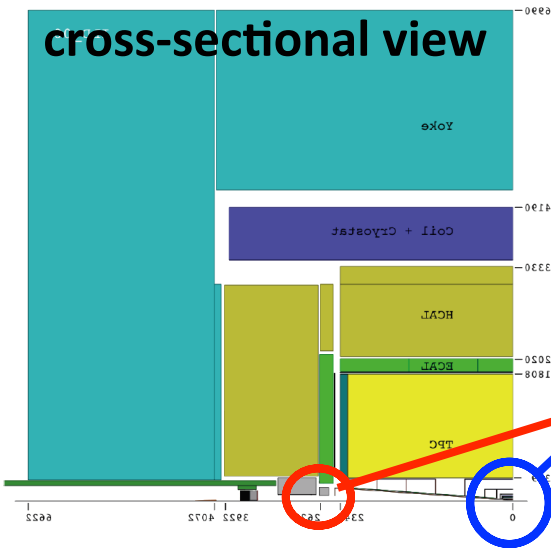


Occupancy

Setup for Pixel Occupancy

we must also take into account background (bkg.) in VXD

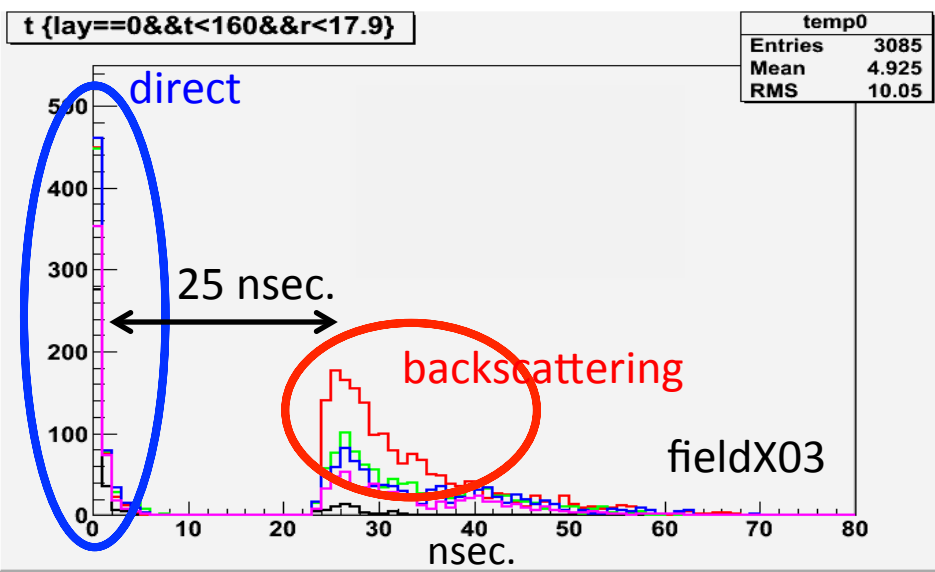
→ dominant bkg. in VXD is derived from the beam



e^+e^- Pair bkg.

→ generated from beamstrahlung at beam collision point

- direct hit
- backscattering from BeamCal (BCAL)



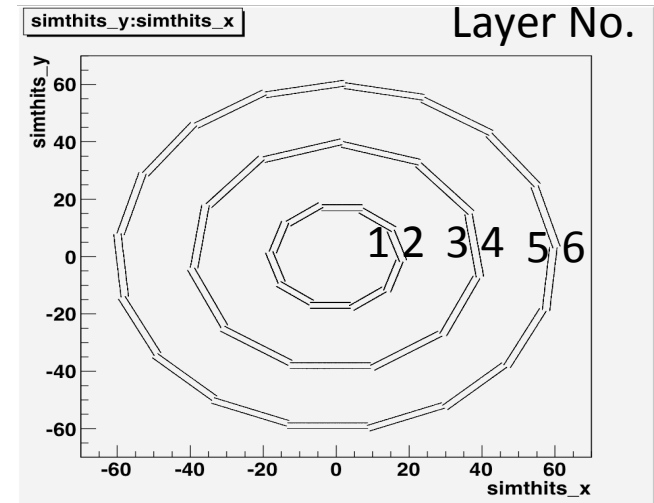
Calculation of occupancy

- 1: Pair bkg. hits from 10 BX are simulated (BX : bunch crossing)
- 2: Create pixel hits by digitizer which takes into account Landau distribution, threshold, path length, noise
- 3: Occupancy is scaled to 1 train

Evaluation of Pixel Occupancy

Requirement : below 2 ~ 3 %

Layer No.	Occupancy(%) at 500 GeV		
	all	direct	backscatter
1(inner)	2.8	1.1	1.7
2	1.6	0.7	0.9
3	0.1	0.0	0.0
4	0.0	0.0	0.0
5	0.0	0.0	0.0
6(outer)	0.0	0.0	0.0



500 GeV is OK!!

Layer No.	Occupancy(%) at 1 TeV		
	all	direct	backscatter
1(inner)	19.6	5.1	14.5
2	10.4	3.1	7.3
3	0.2	0.2	0.1
4	0.2	0.1	0.1
5	0.0	0.0	0.0
6(outer)	0.0	0.0	0.0

However 1 TeV is challenging

Solutions:

- Larger radius
- Make pixels smaller
- Optimize geometry of forward detector
- Reduce bkg. hits using cluster shape

Performance with Larger Pixel Size

Performance with Larger Pixel Size

FPCCD VXD has lots of pixels → large power consumption

Lower power consumption could be achieved by larger pixel size

“small”
“large”

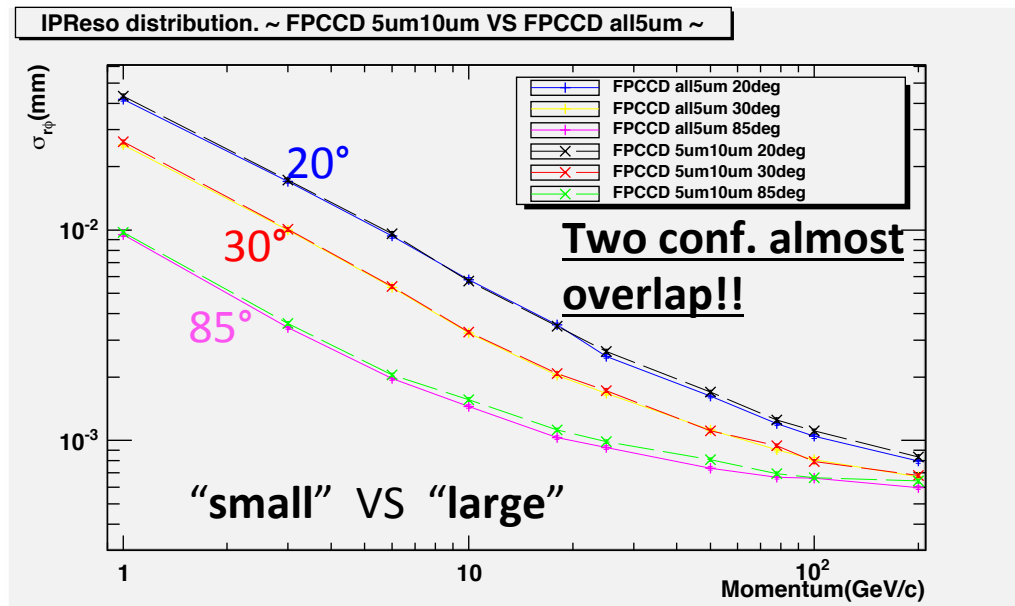
Pixel size (1st ,2nd layer)	Pixel size (outer 4 layers)	Power consumption
5 μm	5 μm ~70%	111 W
5 μm	10 μm reduction!	34 W

Pixel Size	Spatial Resolution
5 μm	1.44 μm
10 μm	2.88 μm

Occupancy and IP resolution with “large” configuration were evaluated

Occupancy(%) at 1 TeV 10 x 10 μm^2			
layer No.	all	direct	backscatter
3	0.5	0.4	0.1
4	0.5	0.3	0.1
5	0.1	0.1	0.0
6	0.1	0.1	0.0

Low Occupancy!



“Large” configuration which can reduce power consumption by 70% satisfies requirement of occupancy and IP resolution

Tracking Performance

Tracking in ILD

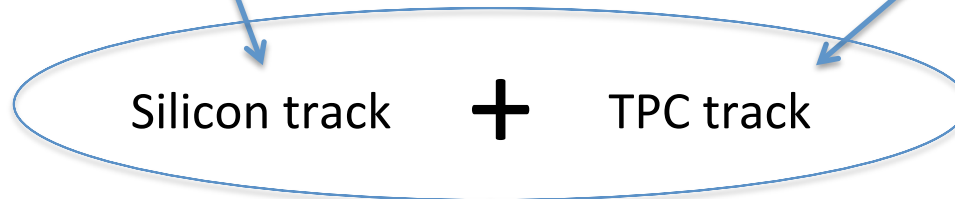
↓ frequently referred from here

1st phase:

Stand-alone silicon (VXD + SIT) tracking

Stand-alone TPC tracking

2nd phase:

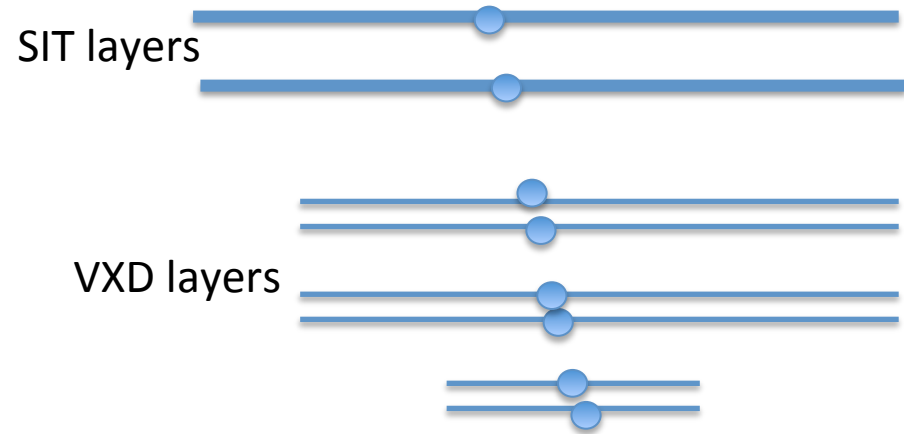


track merging
&
refitting

Merged track

Silicon Tracking Process

load VXD hits



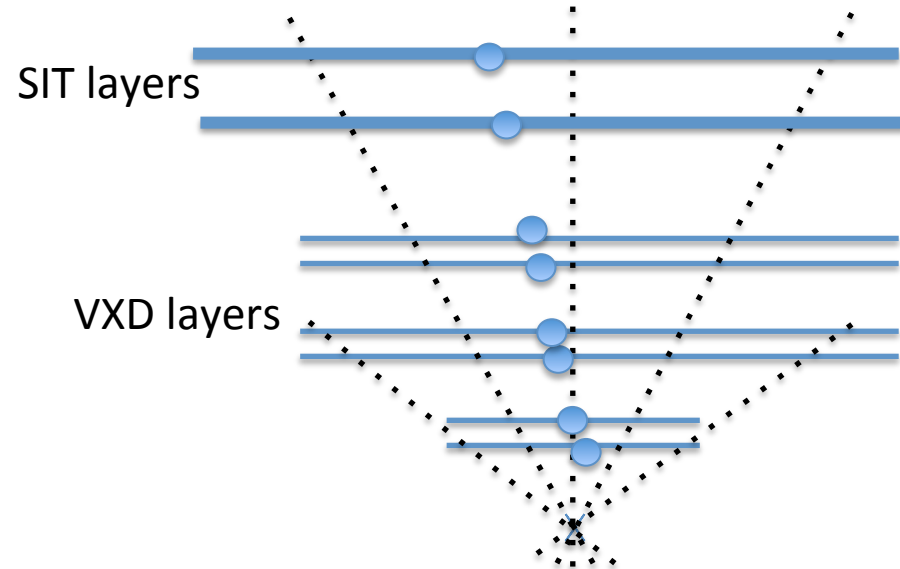
Silicon Tracking Process

load VXD hits



triplet search

→ triplet is track seed



First, we divide the area into $80 \theta \times 80 \phi$ regions

Second, we search the triplet in each area

Silicon Tracking Process

load VXD hits

triplet search

→ triplet is track seed

Third, triplet will be found on seed layers

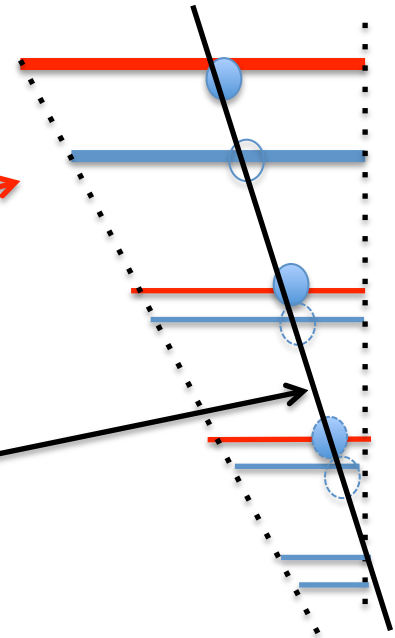
Fourth, triplet will be fitted

At last, if the result of the fit satisfies χ^2/ndf and track parameter requirements, then the triplet becomes the seed of track candidate

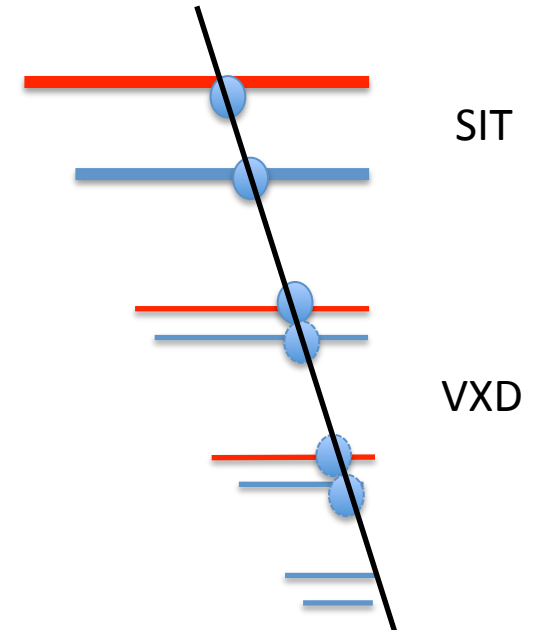
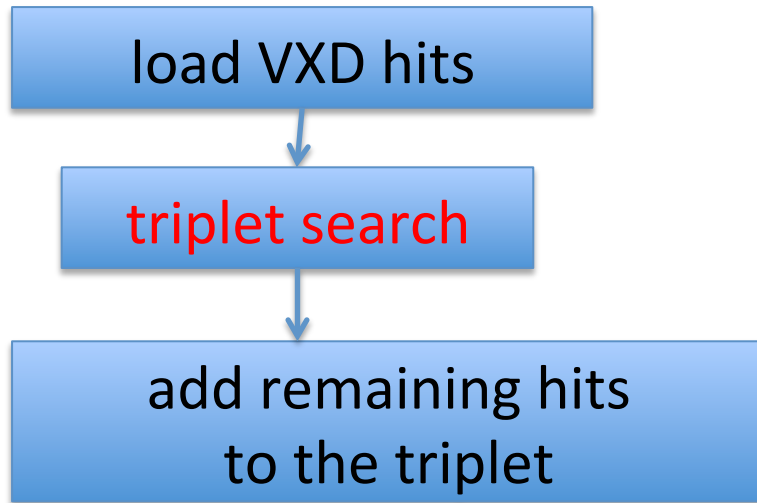
red : seed layers

SIT

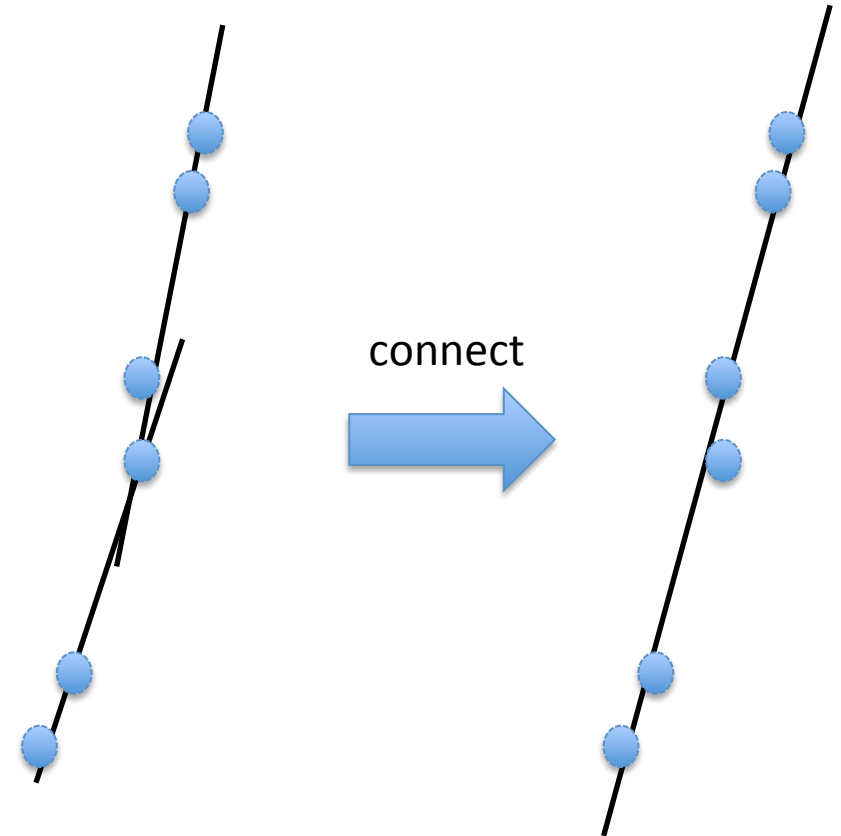
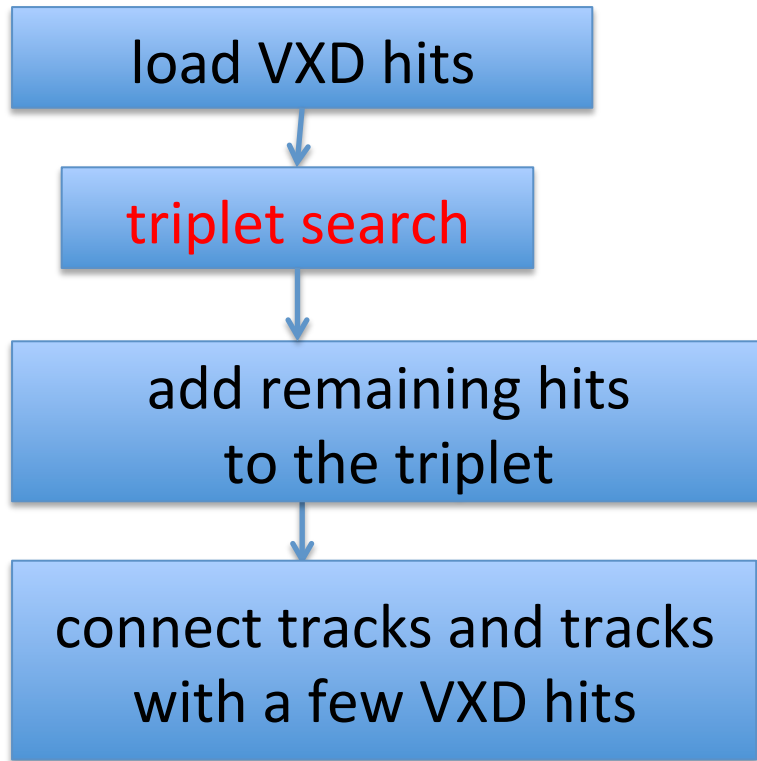
VXD



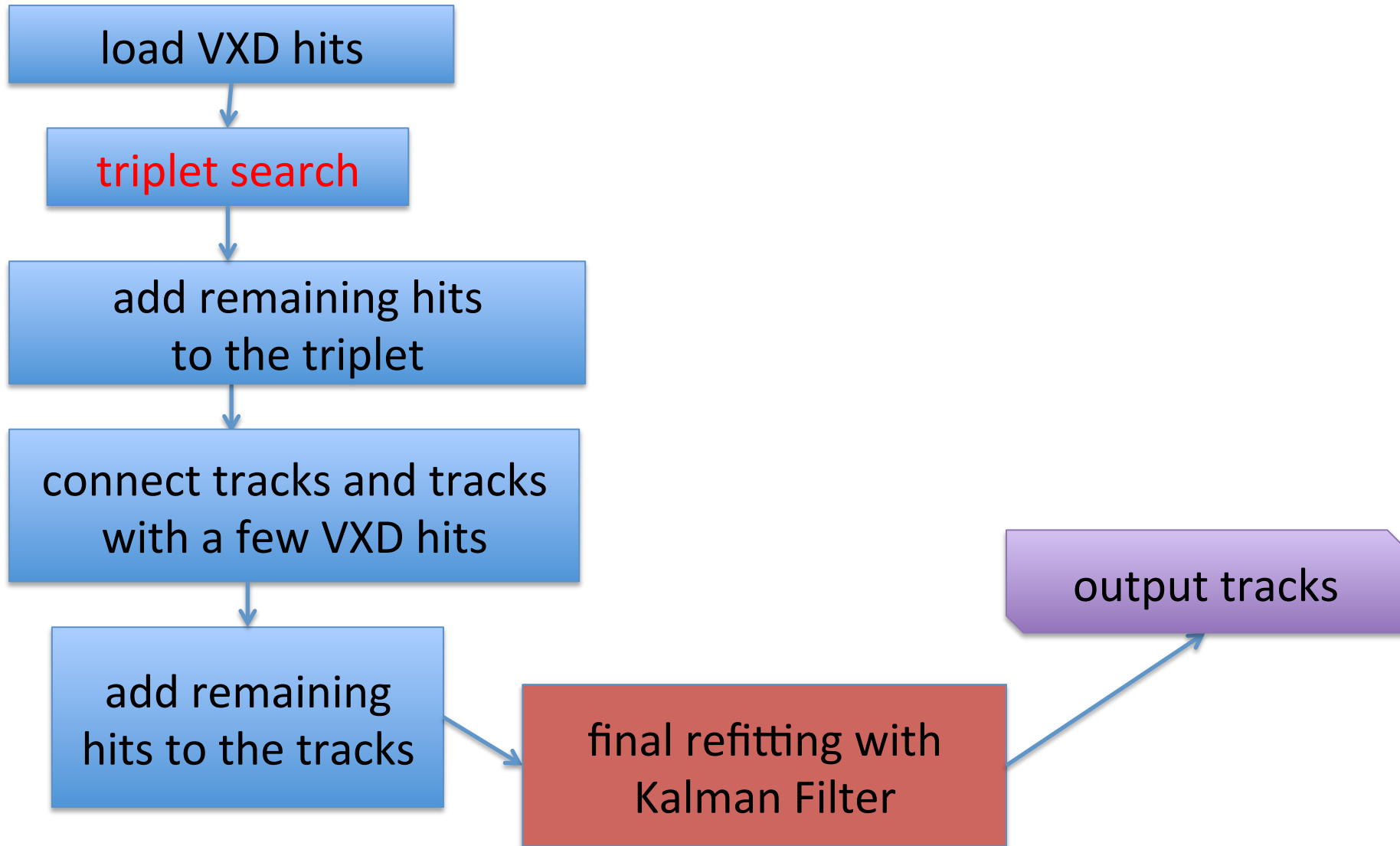
Silicon Tracking Process



Silicon Tracking Process



Silicon Tracking Process



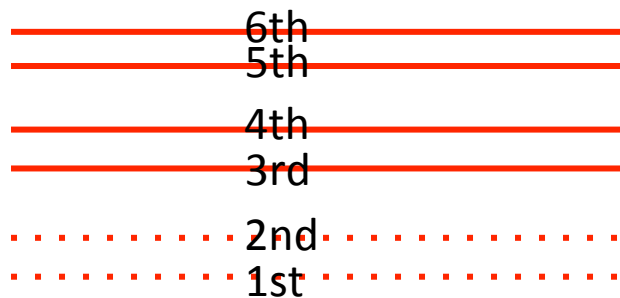
Challenge of Tracking with Pair bkg.

There are many bkg. hits in two most inner layers of FPCCD VXD
If they are included in the triplet search, there will be many fake triplets and
we consume a lot of CPU time for many combinations



We studied tracking performance **excluding two most inner layers**
from triplet search

FPCCD VXD layers :



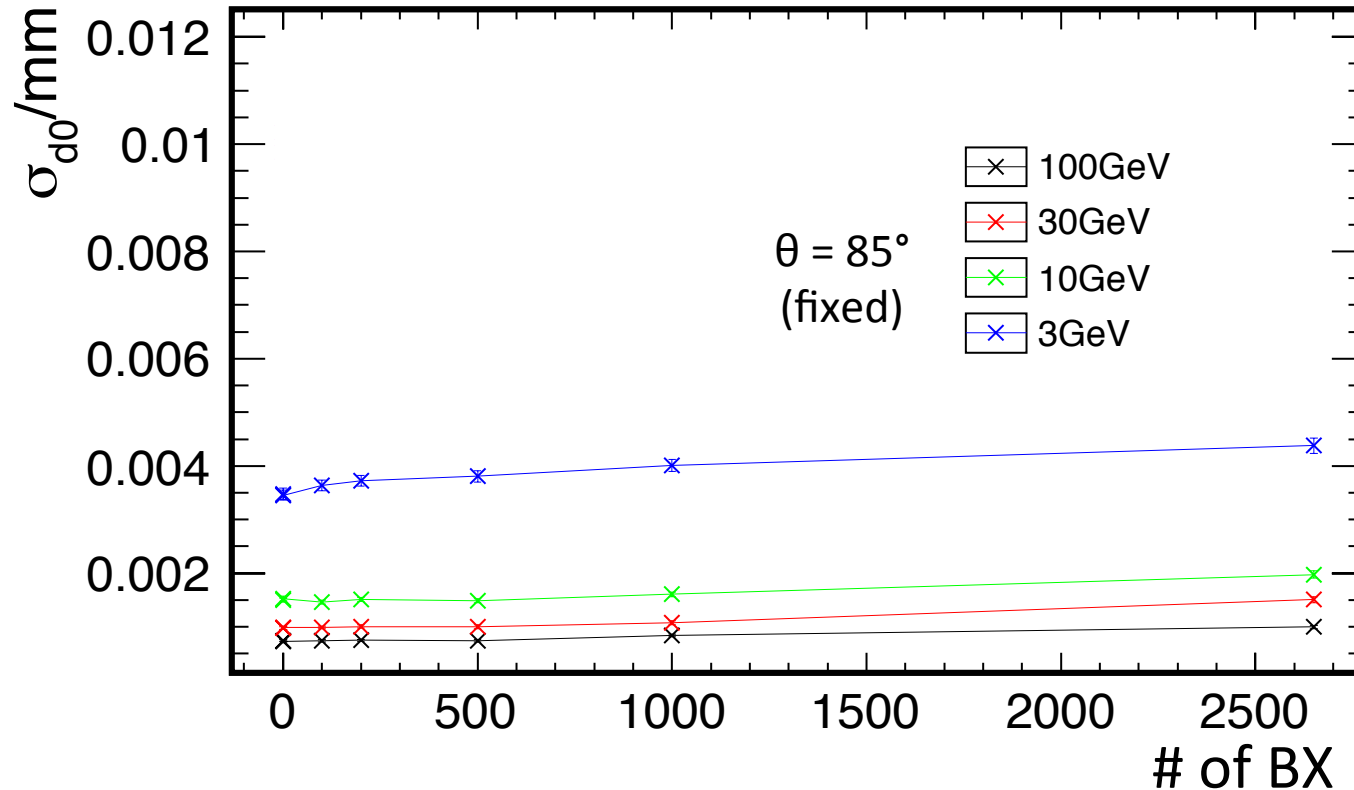
} not used for triplet search
in this study

Setup for evaluation of tracking in FPCCD:

- Pair bkg. in 1TeV beam run is overlaid on single μ^+ event
Pair bkg. from 1, 100, 200, 500, 1000, 2650 BX (= 1train) are studied

Evaluation of IP Resolution of Good Tracks with bkg.

Good Track \equiv track with VXD hits ≥ 5



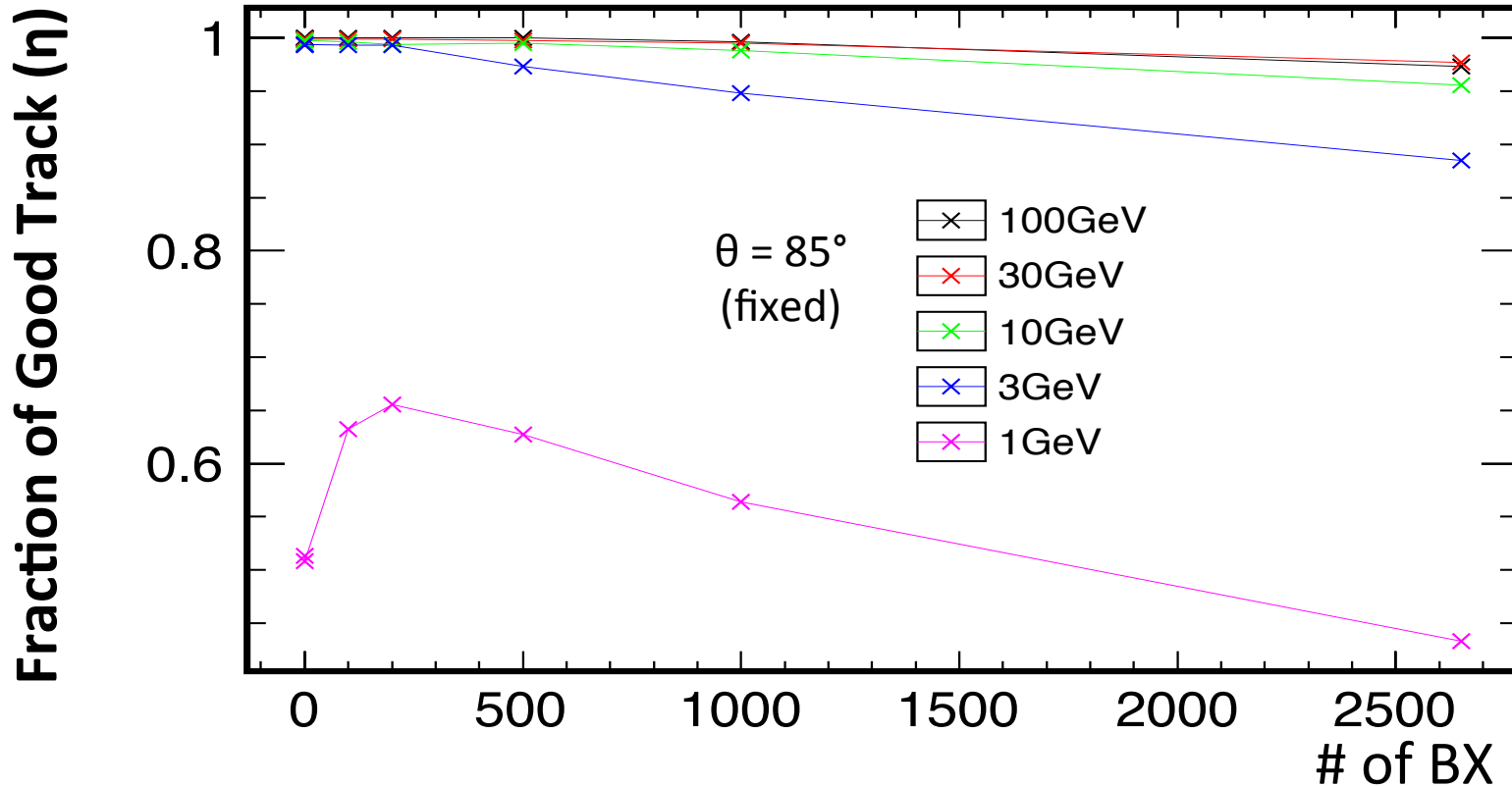
IP resolution of good tracks is EXCELLENT

&

Deterioration of resolution is small

Evaluation of Fraction of Good Track

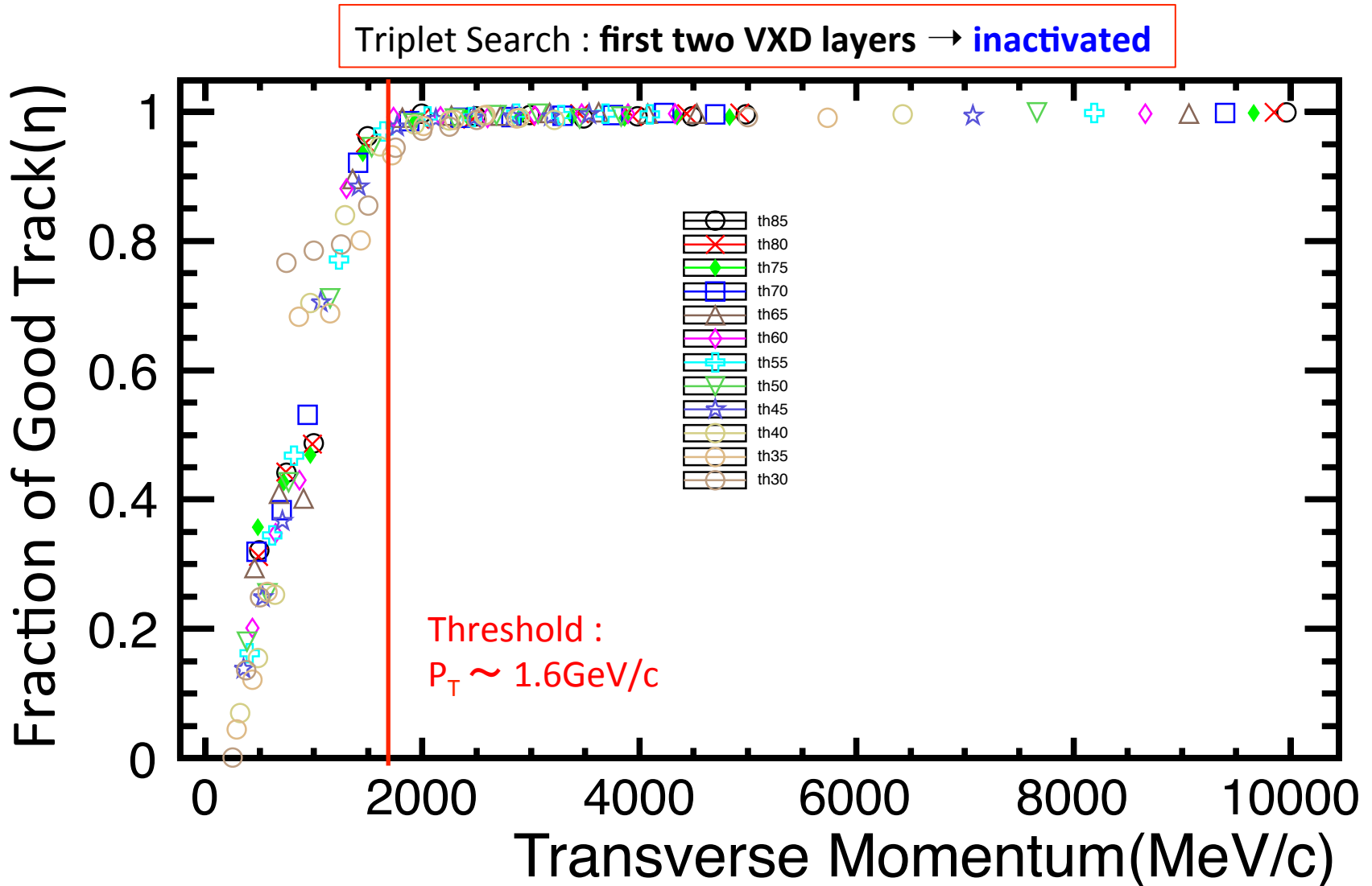
$$\text{Fraction of Good Track : } \eta \equiv \frac{\text{\# of tracks with VXD hits } \geq 5}{\text{\# of } \mu^+ \text{ with 6 VXD hits in simulation}}$$



→ A problem in tracking of 1 GeV particle

Threshold of track deterioration in FPCCD

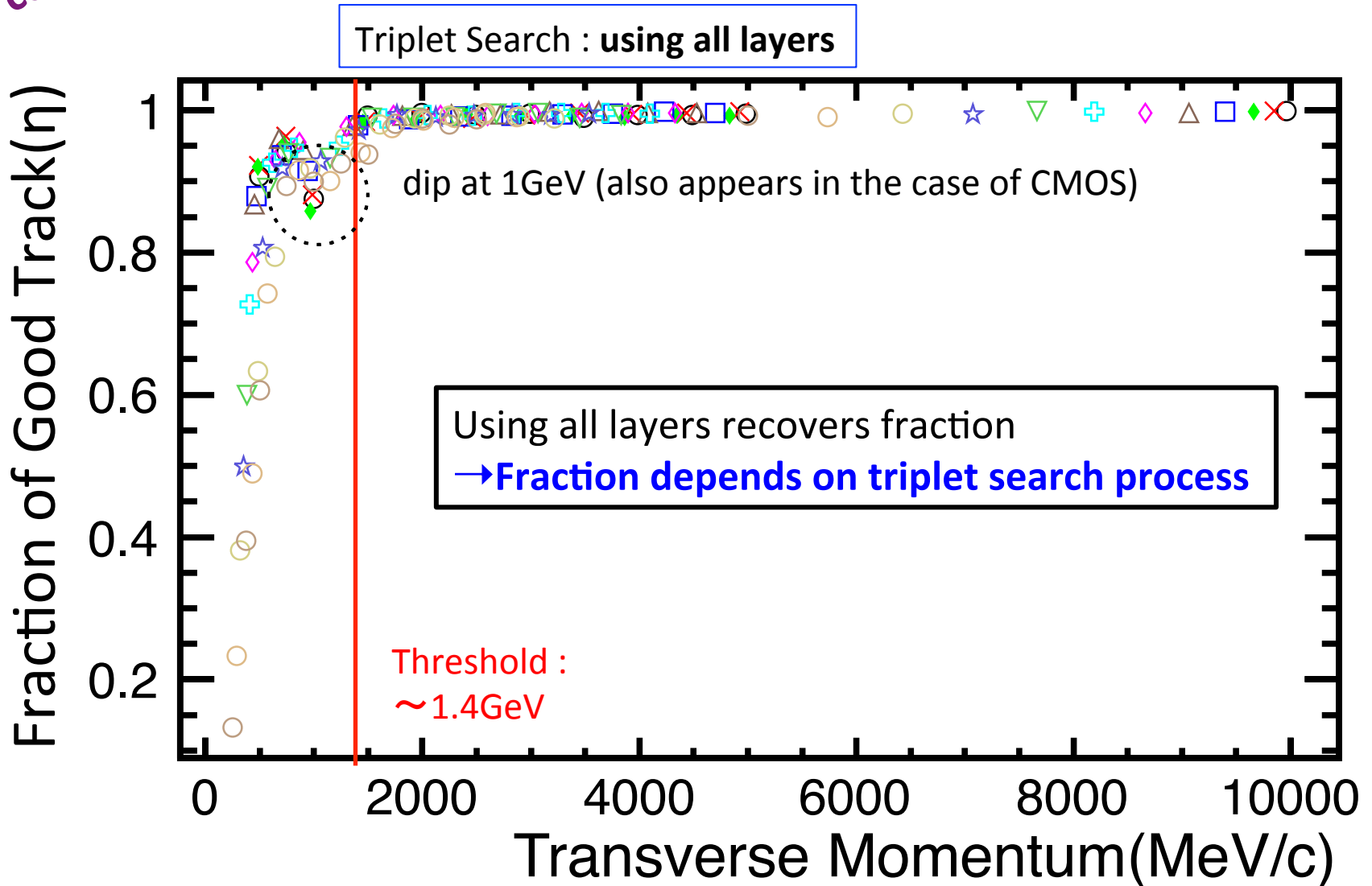
without pair bkg.



Threshold of track deterioration in FPCCD

without pair bkg.

For comparison



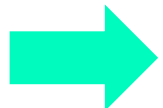
ϕ Division in Silicon Tracking

- Most preferred triplet search combination : **SIT's two and VXD's outermost layers**
→ for avoiding picking up beam background hits
- In standard configuration, search area is divided into 80 x 80 (θ and ϕ)
→ **too strict to find triplets in preferred layers**

If # of ϕ divisions is reduced, efficiency of silicon track increases.

ϕ division	fraction of good track in stand-alone silicon tracking
80 (default)	5%
40	22%

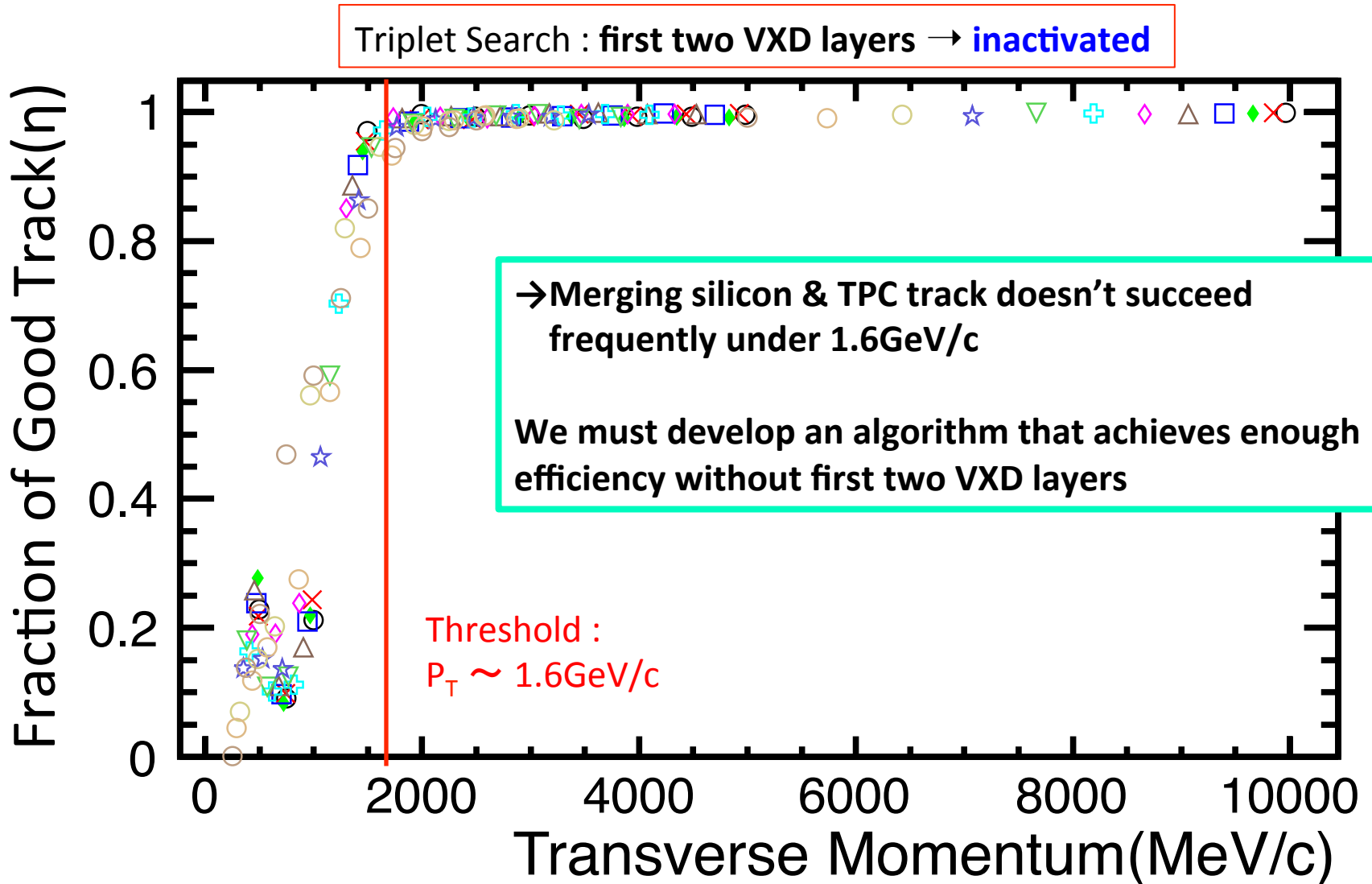
(evaluated with single μ^+ event, $|P| = 1\text{GeV}/c$, $\theta = 85^\circ$)



By 40 ϕ division, efficiency of merged track is expected to increase

Efficiency of Merged Track (ϕ division of 40)

However, in spite of improved efficiency of silicon track,
fraction of good track becomes a little worse



Summary

Occupancy:

- Pixel occupancy : **Good!!** (under $E_{CM} = 500$ GeV)

Performance with Larger Pixel Size:

- Configuration of pixel size $10\mu\text{m}$ in outer 4 layers leads to **70%** reduction of power consumption
→ while keeping pixel occupancy and IP resolution requirement satisfied

Tracking Performance:

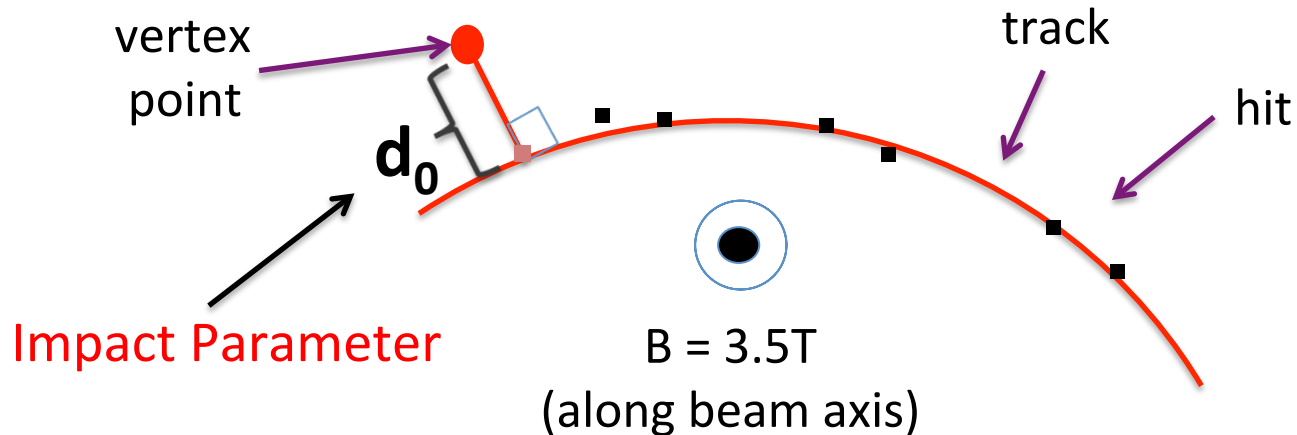
- Fraction of Good Track : **Good!!** (except low P_T)
- IP resolution under pair bkg. : **Good!!**
- Need improvements of low P_T tracking efficiency

BACK UP

Requirement : Impact Parameter Resolution

The higher impact parameter resolution (IP resolution) VXD has, the more precise the separation between b, c, and g is

Definition of IP resolution:



**IP resolution
requirement**

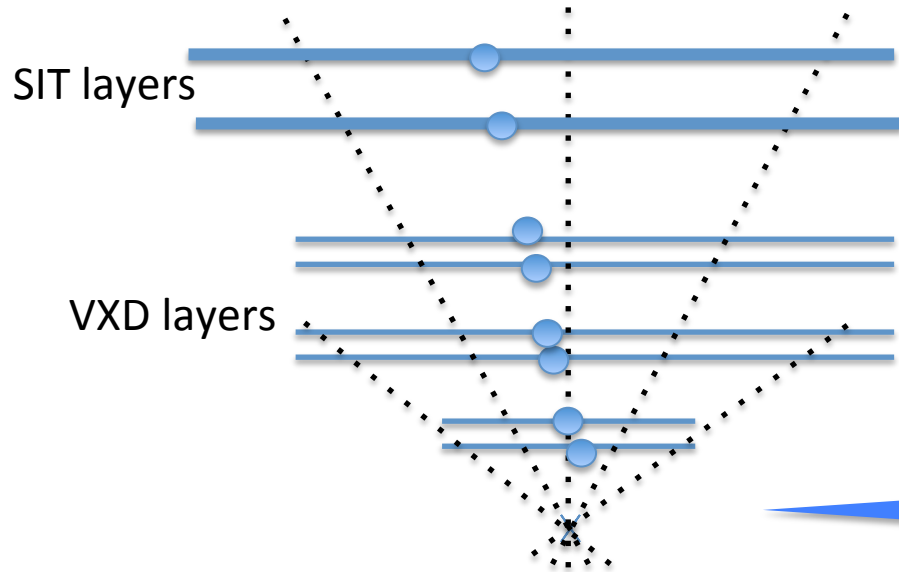
$$\sigma_{r\phi} = 5\mu\text{m} \oplus \frac{10\text{GeV}/c}{p \cdot \sin^{3/2} \theta} \mu\text{m}$$

p : absolute momentum[GeV/c], θ : angle from beam axis

Parameterization of Digitizing for Evaluating Occupancy

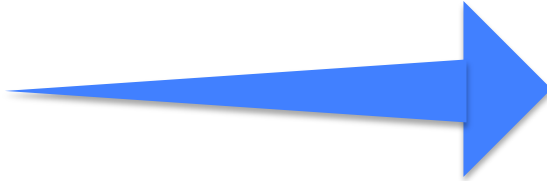
1. From path Length, energy deposit is calculated
2. The energy deposit is smeared by Landau distribution with $\sigma = 32000 \times \text{“path Length”}$
3. We assume 276 electrons per 1KeV in a pixel
4. The threshold of energy deposit : $> 0.72\text{KeV}$
(corresponding to 200 electrons)
5. The energy deposit is also deposit by Gaus distribution with $\sigma = 0.18\text{KeV}$ (corresponding to 50 electrons)

Triplet Search Process



First, we divide the area into $80 \theta \times 80 \phi$ regions

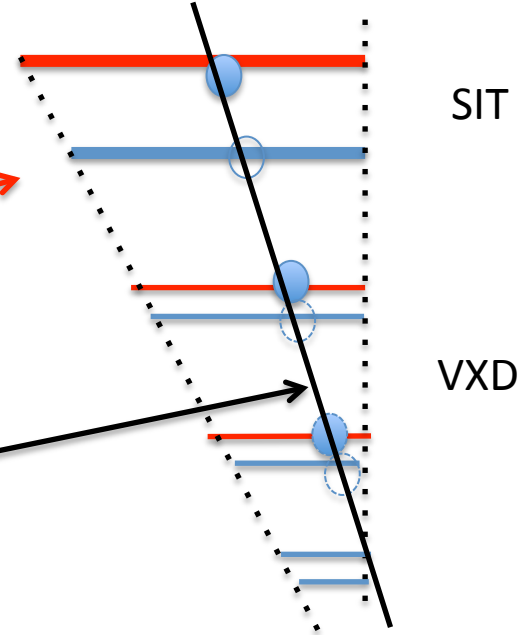
Second, we search the triplet in each area



red : seed layers

Third, triplet will be found on seed layers

Fourth, triplet will be fitted



At last, if the result of the fit satisfies Chi^2/ndf and track parameter requirements, then the triplet becomes the seed of track candidate

Setup for Threshold of Track Deterioration

Threshold of track deterioration was investigated with following setup

Setup :

- Digitizer : VXDPlanarDigiProcessor
 - spatial resolution : $1.44 \mu\text{m}$ in all layers
 - resolution of FPCCD

- only one μ^+ in one event

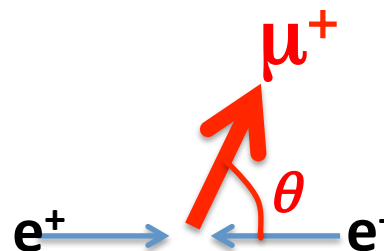
- polar angle with respect to beam axis :
 $\theta = 85 \ 80 \ 75 \ 70 \ \dots \ 35 \ 30^\circ$

- Absolute Momentum :

10000 5000 4500 4000 3500 3000 2500 2000 1500 1000 750 500 MeV

- Triplet Search :

VXD inner two layers **inactive** for beam bkg.



One Reason for Track Deterioration

Question : When are VXD hits assigned to a track lost?

- silicon tracking phase?
- merging Silicon & TPC track phase?

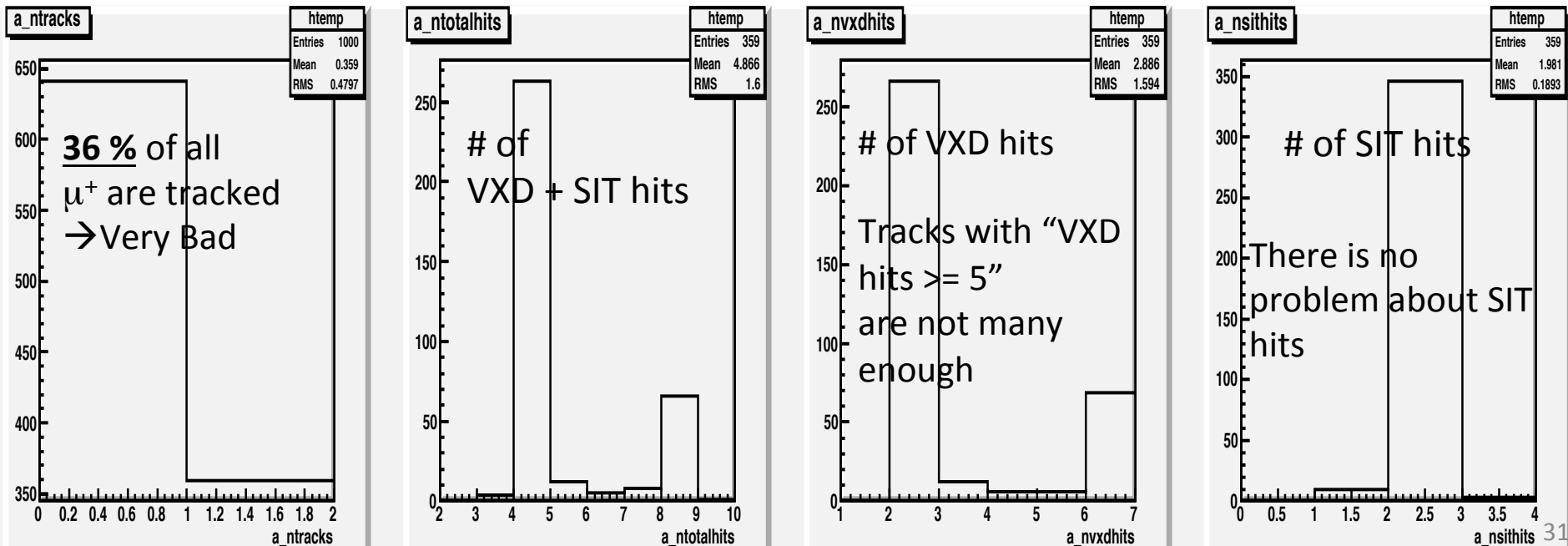
One Answer : silicon tracking phase

Setup for checking tracking efficiency in silicon tracking

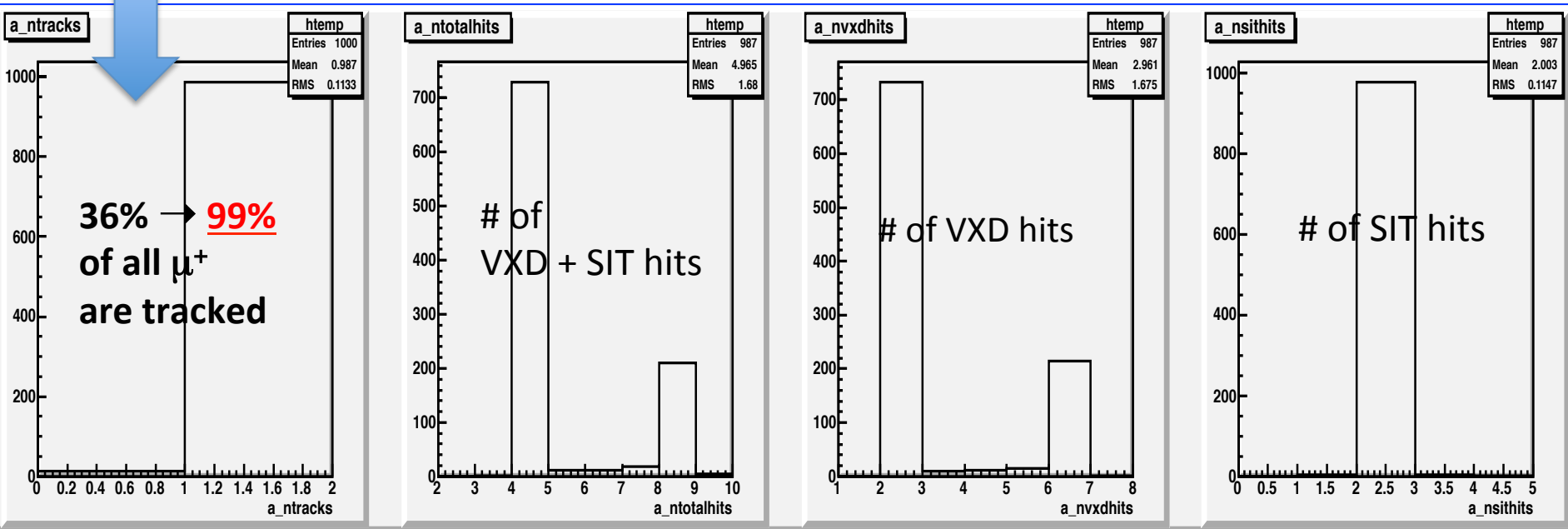
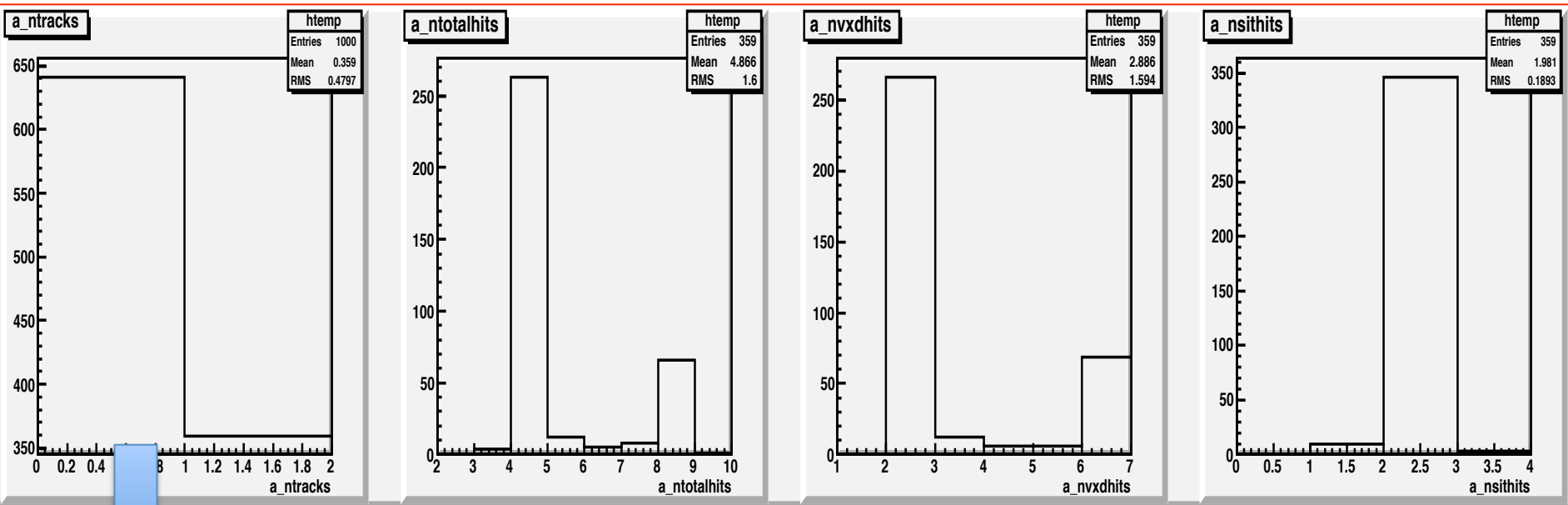
single μ^+ event, $|P| = 1\text{GeV}/c$, $\theta = 85^\circ \rightarrow 1000\text{events}$

Active tracker : silicon tracking (only)

Triplet Search : not using VXD inner two layers for beam bkg.



strict division(80 x 80, default)

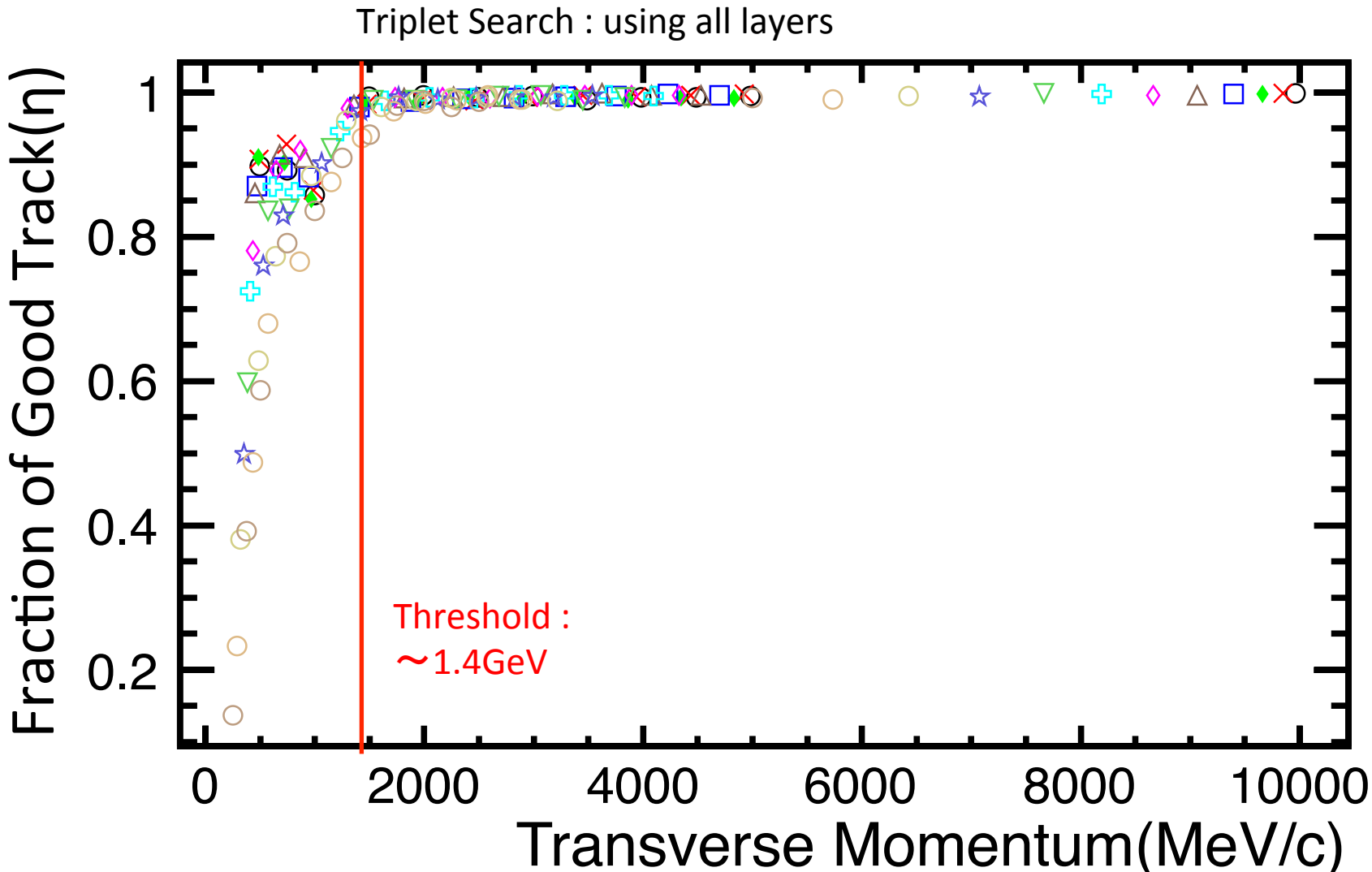


loose division(80 x 40)

→ Tracking efficiency increases much.

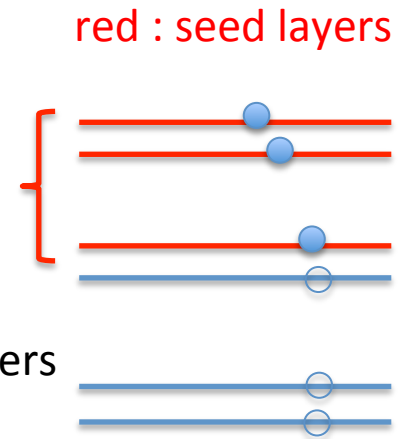
ϕ -division 40

Fraction of good track using all layers also becomes a little worse



Other Possible Improvements

- Add triplet search combination of continuous VXD layers



- Add new way of “addition of remaining hits to triplets”
- Optimize fit requirement for χ^2/ndf and track parameters