Development of Readout ASIC for FPCCD Vertex Detector

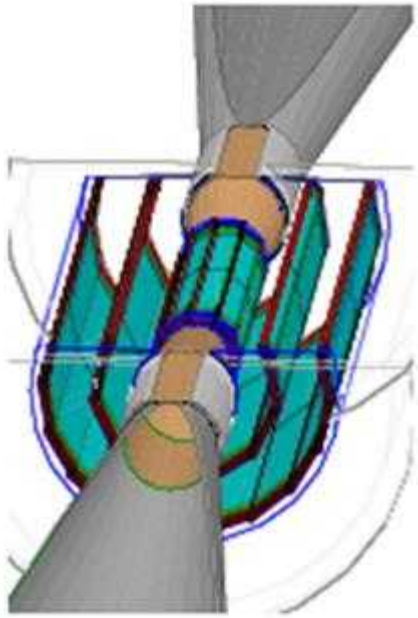
2009.4.20

Kennosuke.Itagaki

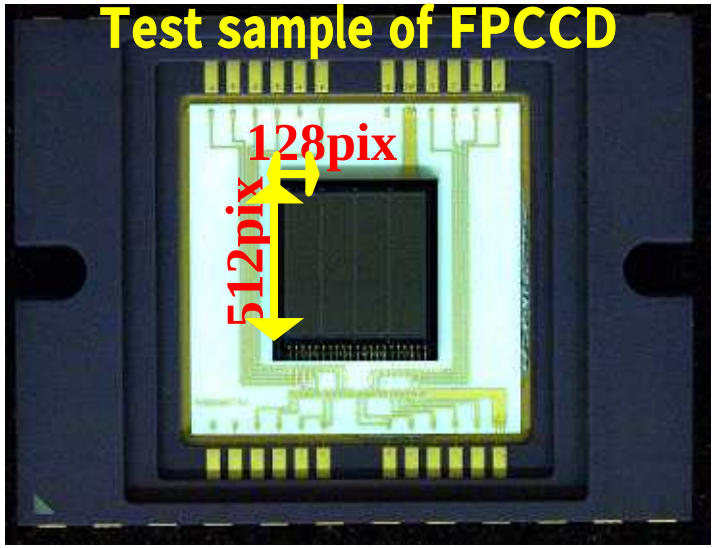
Tohoku University

FPCCD Vertex Detector

- Fine Pixel CCD Vertex Detector
  - Pixel size：5μm × 5μm
  - Thickness of epitaxial layer：15μm
  - Ladder size：12cm × 1cm
  - # of readout channel：～6,000ch
    - ➢20,000 × 128 pix/ch



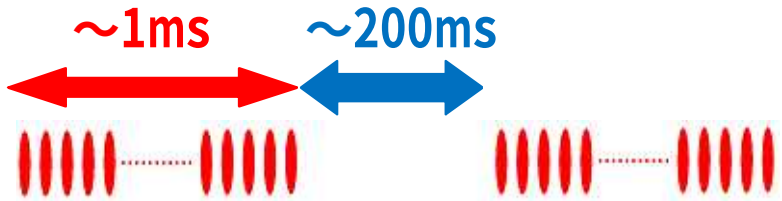
- Test sample for establish technology
  - Delivered in March 2008
  - Pixel size：12μm × 12μm
  - Thickness：15μm,24μm
  - # of readout channel：4ch
    - ➢512 × 128 pix/ch



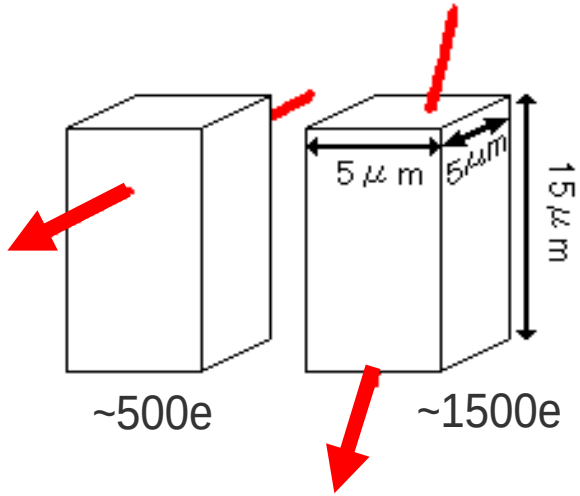
➢ Readout ASIC was developed

Requirement to readout ASIC

- Readout rate > 10 Mpix/sec
  - ➢ Readout in the inter train time
  - ➢ 20,000 x 128pix / 200ms ~ 10Mpix / sec



- Noise level < 30 electrons
  - ➢ Small signal level : ~ 500 electrons
  - ➢ Required noise level with CCD : <50e
    - ✓ Noise level in FPCCD : ~30e

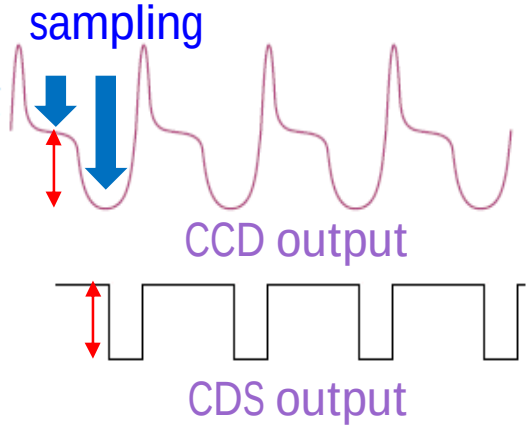


- Power consumption < 6 mW/ch
  - ➢ Vertex detector is in a cryostat

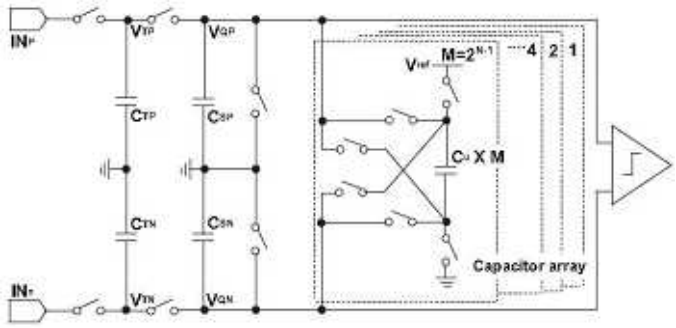
⇨ Readout ASIC was designed to satisfy these requirements

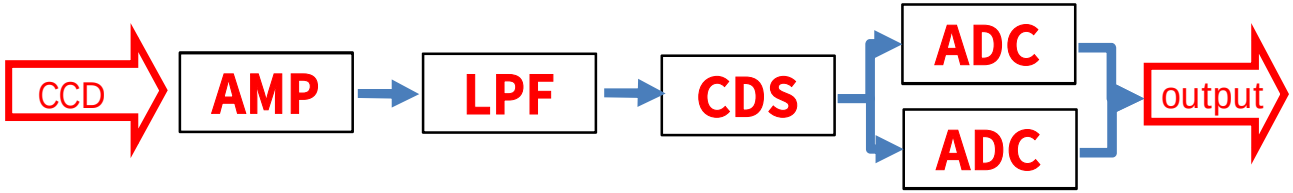
Design concept of readout ASIC

- Amplifier
- Low pass filter (LPF)
- Correlated double sampling (CDS)
  - CCD：Charge in each pixel is output as a voltage difference
  - CDS：Output voltage difference at sampling point
- Charge sharing ADC
  - comparing stored charge in capacitor by input voltage and reference voltage
    - ⇨ power consumption < 10μW/ch
  - 5MHz × 2
  - Serial output



Charge sharing ADC

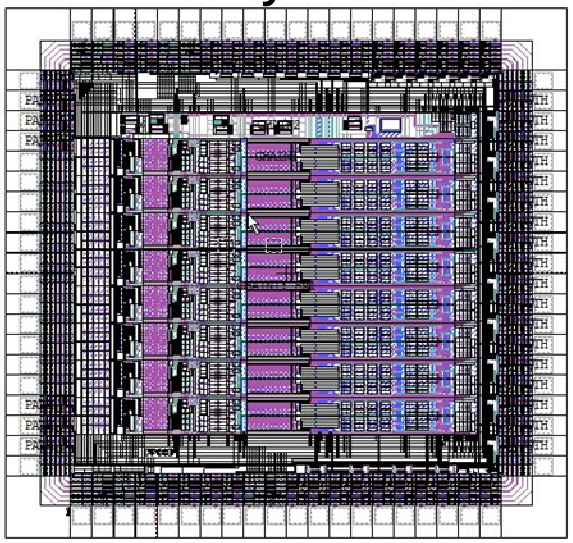




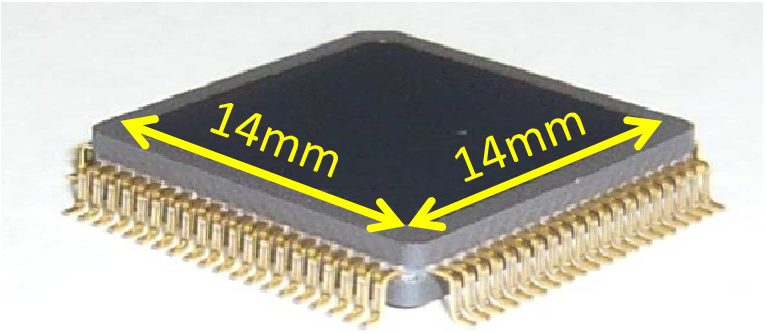
Prototype ASIC

- Delivered in January 2008
- 0.35μm TSMC process
- Chip size：2.85 mm × 2.85 mm
- # of pad：80
- # of readout channel：8
- package：QFP-80 pin

Layout



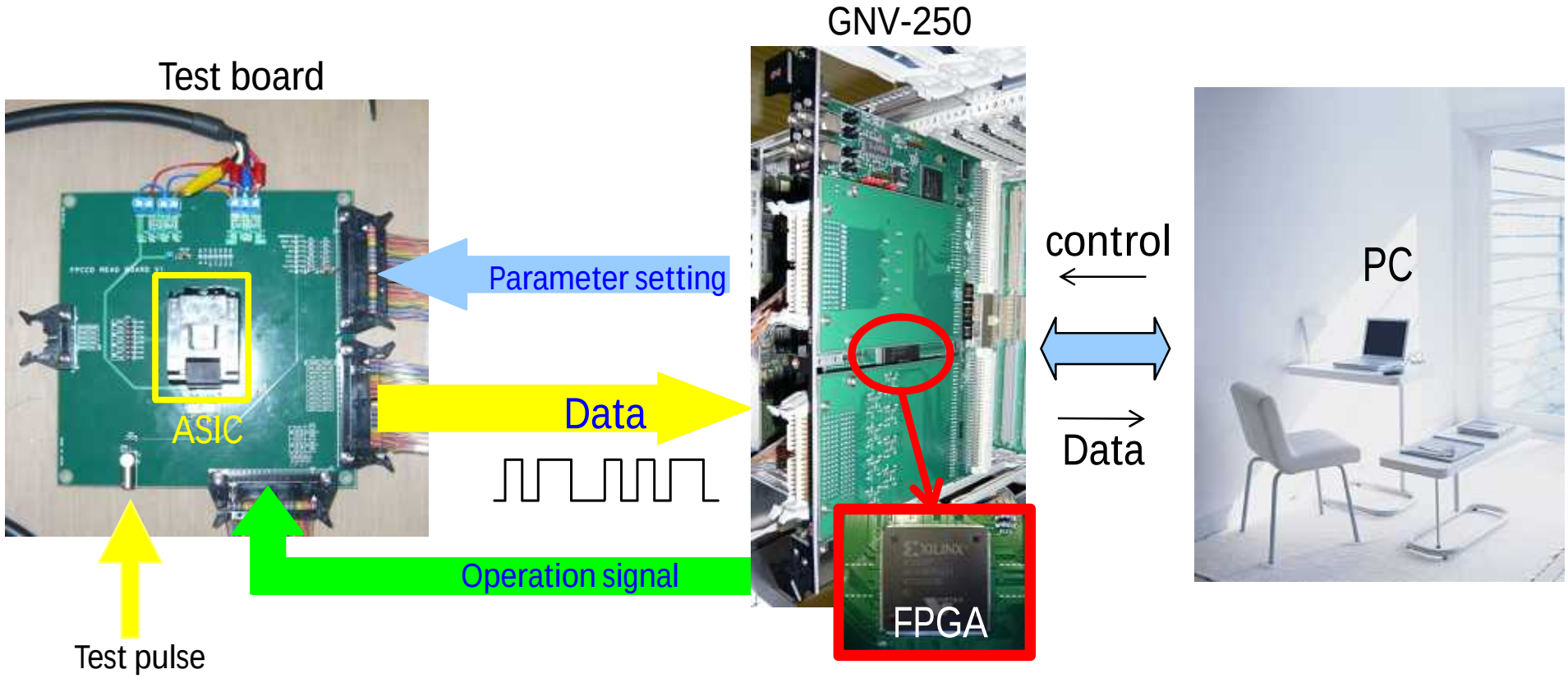
Prototype ASIC with a package



⇨ The performance of prototype was checked

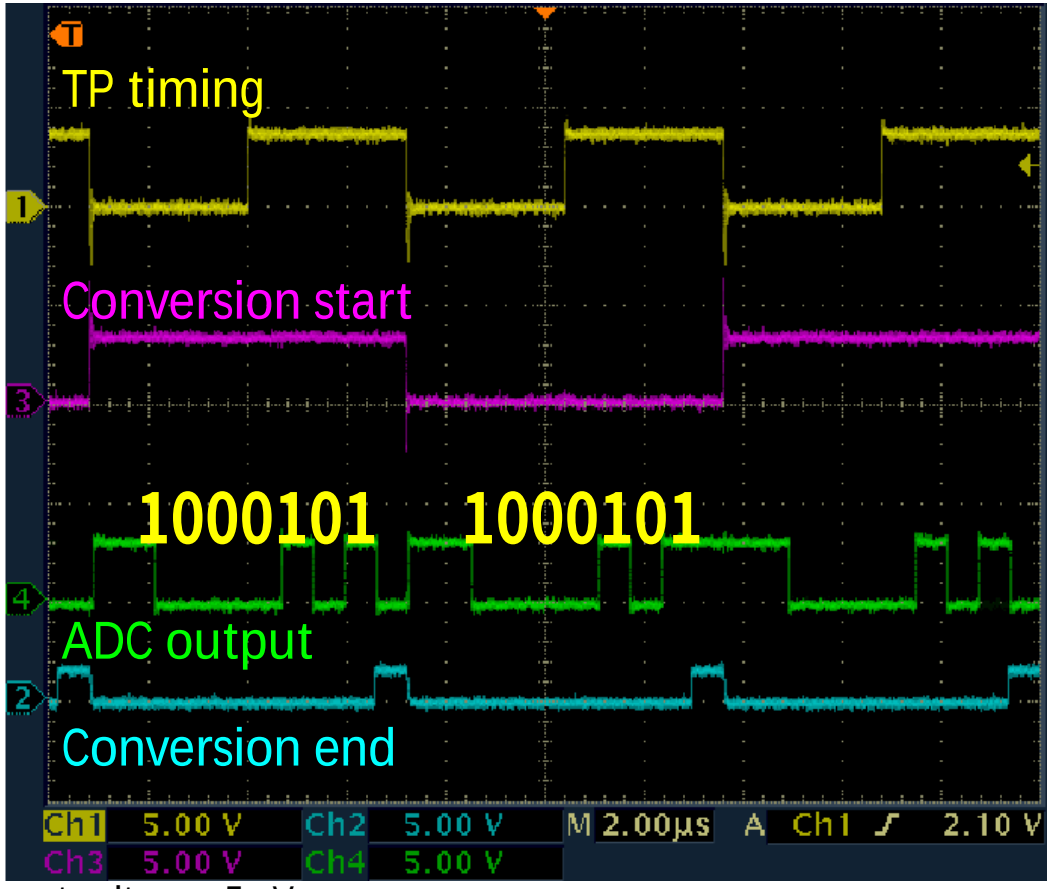
Test bench of readout ASIC

- Data acquisition and circuit control are done by VME module
  - GNV-250 module
  - FPGA is equipped →The control logic was developed
  - The test job and parameter setting are controlled by PC
  - ADC output is stored in FIFO, and sent to PC

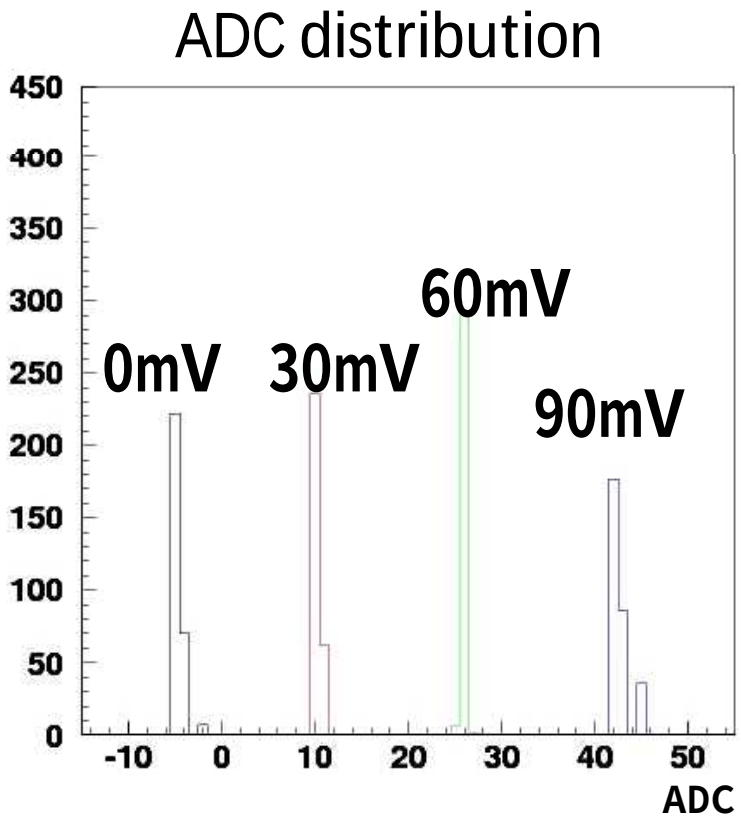


Check of ADC response

- ADC response was checked with conversion rate of 10kpix/sec.



Input voltage～5mV

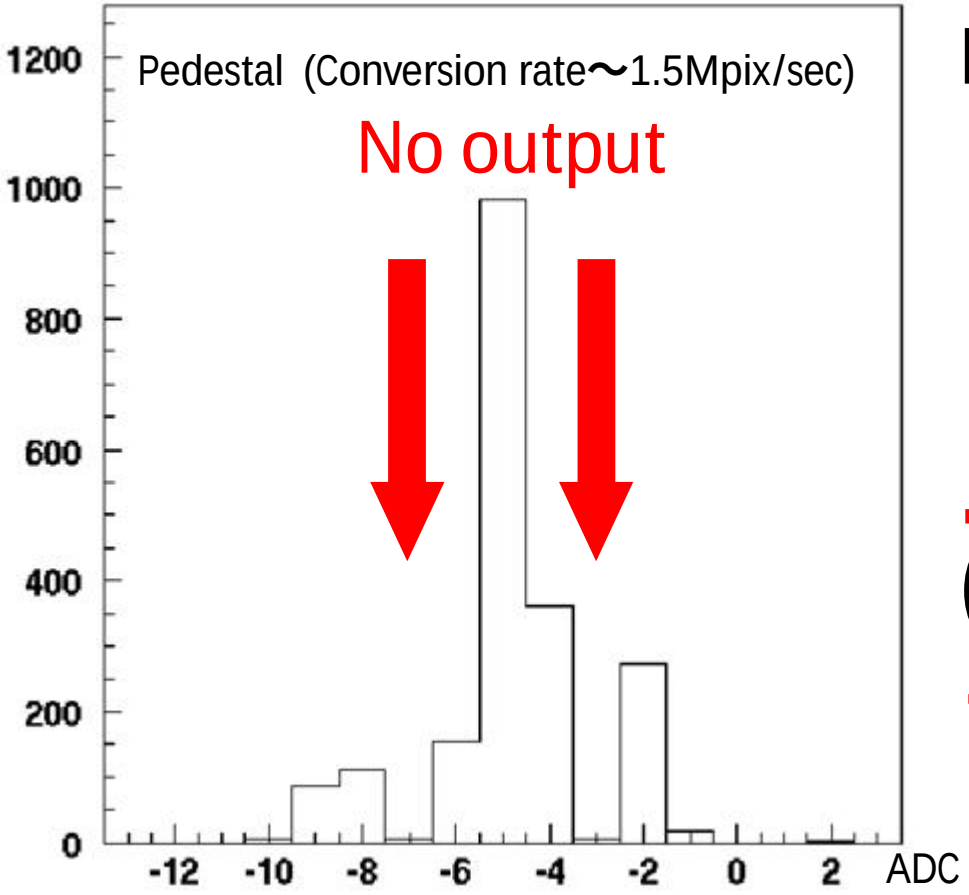


- ADC output is synchronized with the timing of operation signal.

➪ Performance of prototype ASIC was studied.

Noise level

• The pedestal distribution was checked to investigate the noise level, with conversion rate of 1.5Mpix/sec.



Noise

σ ～1.7 ADC count

- **1ADC count ～0.2 mV (at sensor input)**
- **FPCCD : 5μV/e**

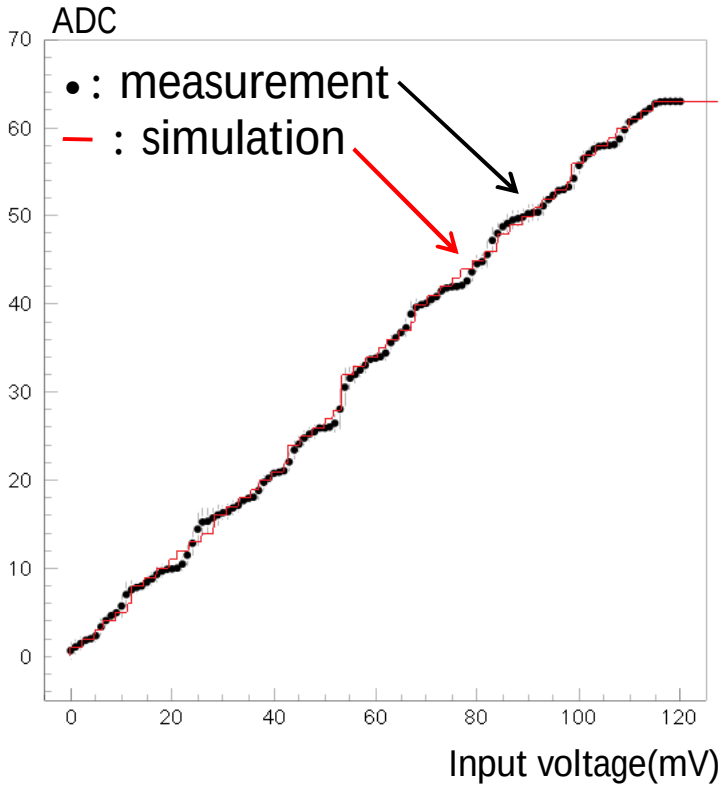
➔Noise level ～70e
(requirement：＜ 30e)

⇨ Necessary to improve

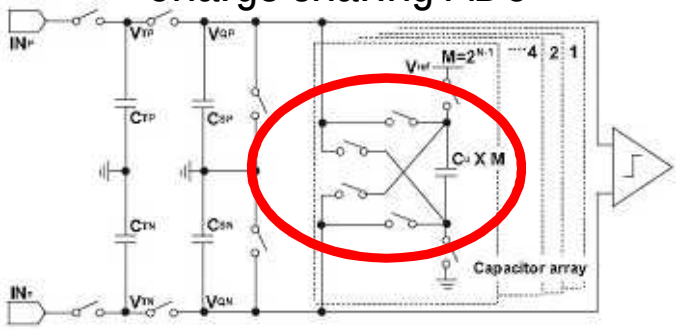
- Some ADC counts are not output from ADC
  - ➢The reason was investigated

Problem in ADC design

- The reason to have the missing ADC count was checked.
- The ADC capacitor ratio is unbalanced by the floating capacitance at the switching circuit in the ADC.



Charge sharing ADC



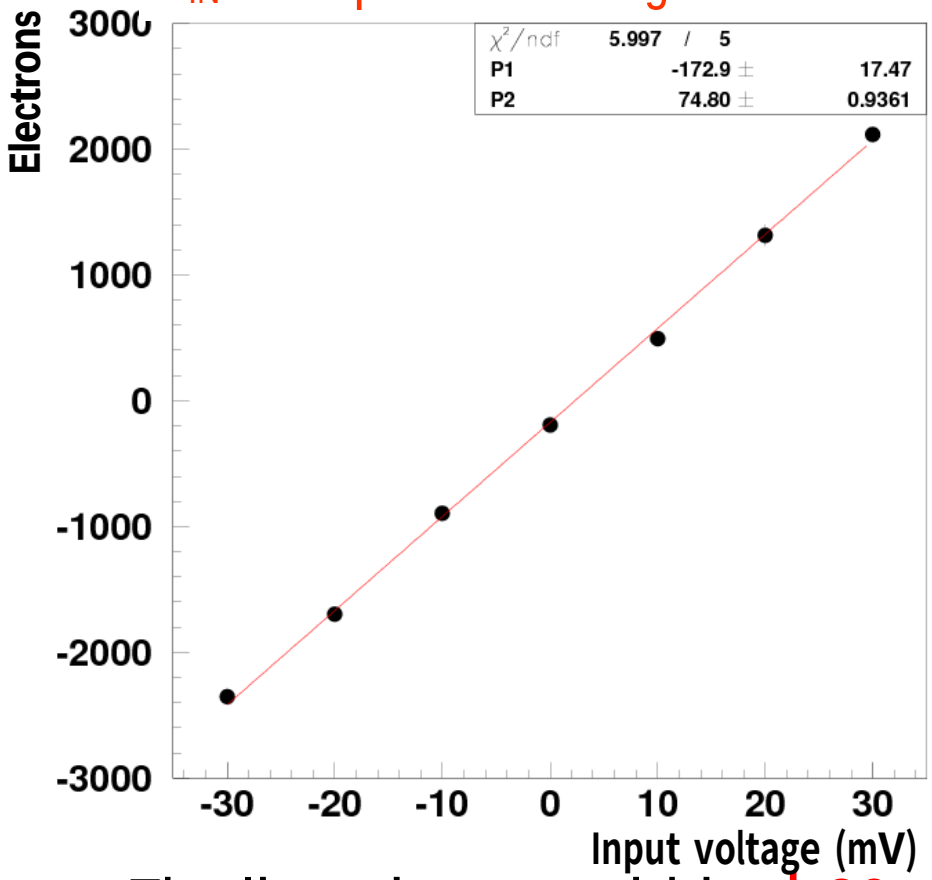
- ADC output was simulated by MATLAB.
- The simulation result for enlarged capacity of each capacitor is consistent with measurement.

⇨ The problem will be improved, adjusting the size of the switching circuit according to each capacitor capacitance.

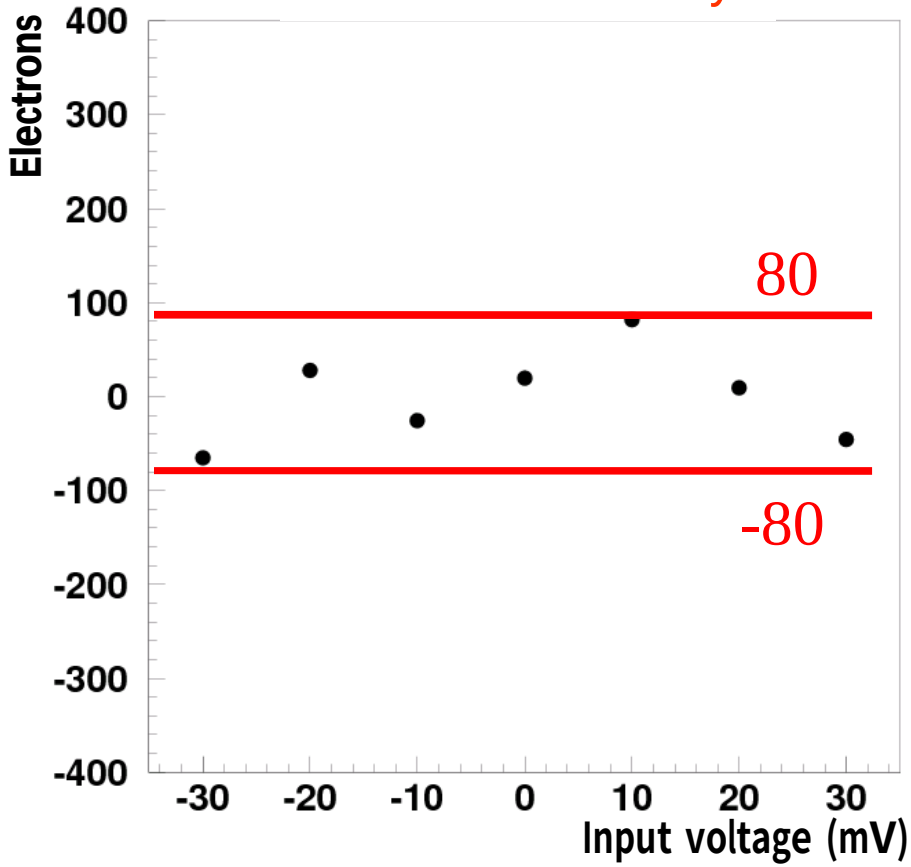
ADC linearity

- The ADC linearity was checked, changing input voltage of the test pulse

V_{IN} v.s. Equivalent charges in FPCCD



V_{IN} v.s. ADC linearity

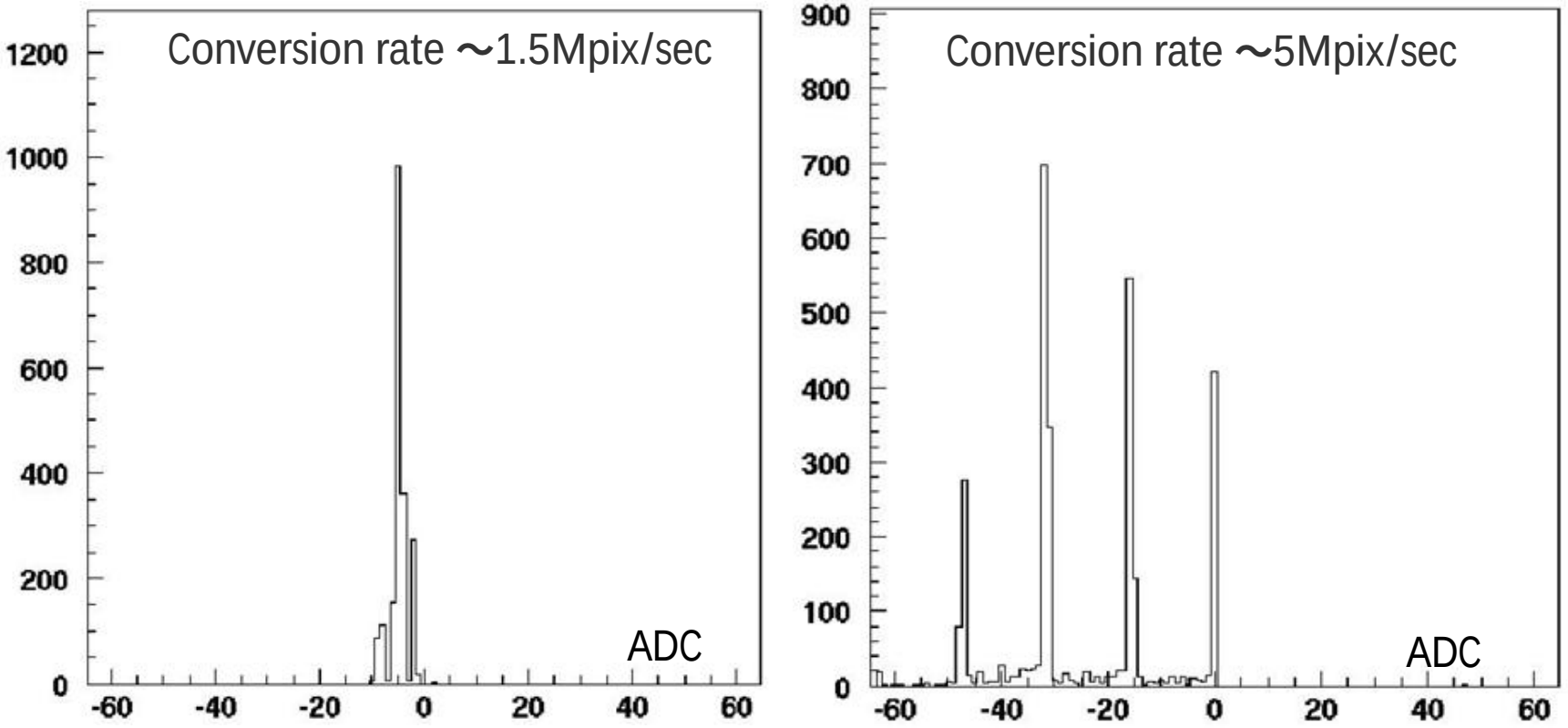


- The linearity was within ±80e

➪ The ADC linearity will be improved by modification of the capacitance of the ADC capacitor.

Test with high speed readout rate

Pedestal



- Final goal：10Mpix/sec
  - ➢ The pedestal distributions have some peaks for 5Mpix/sec

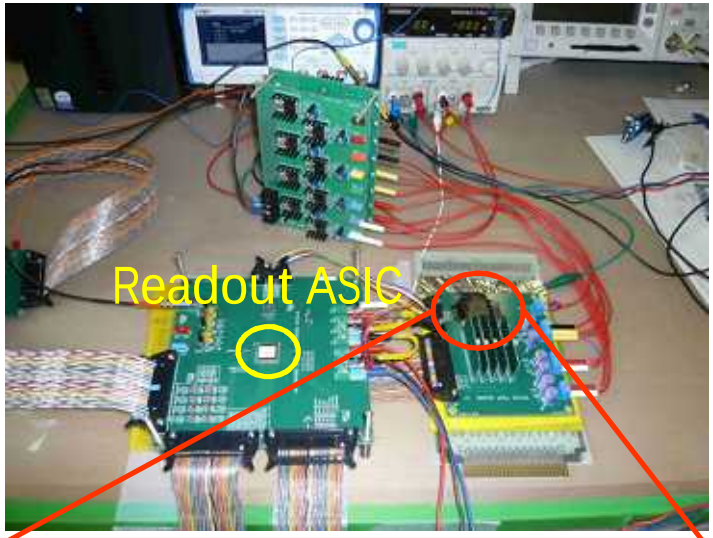
⇨ It will be confirmed by the SPICE simulation

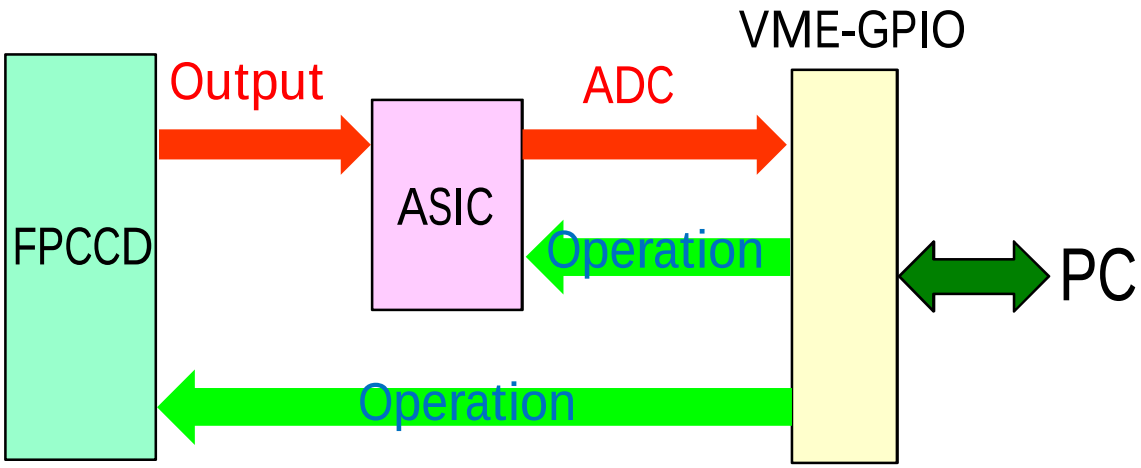
Readout from FPCCD test-sample

The readout from the FPCCD test-sample was started

- The FPCCD test-sample was connected to the prototype ASIC.
- FPCCD is operated by GNV-250 module.

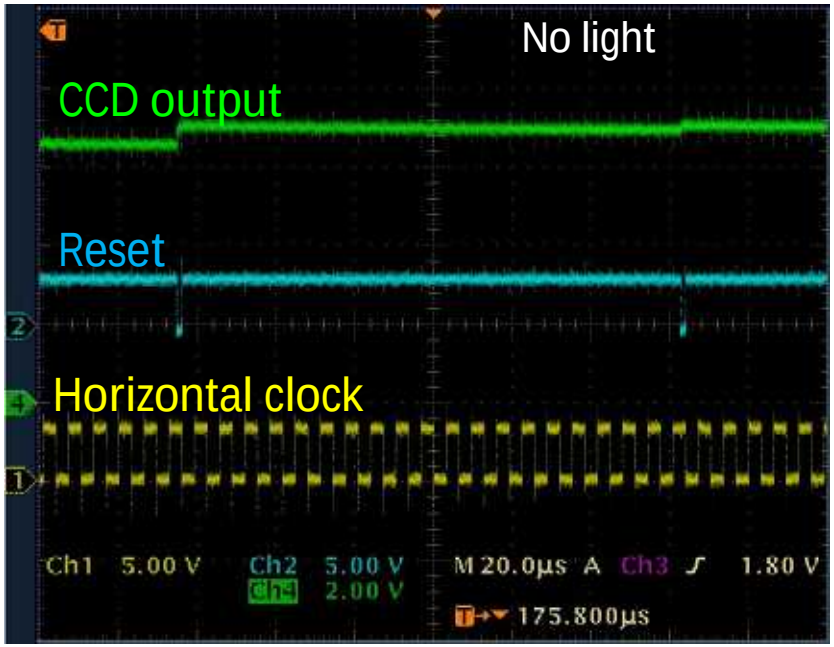
⇨ FPCCD output was checked

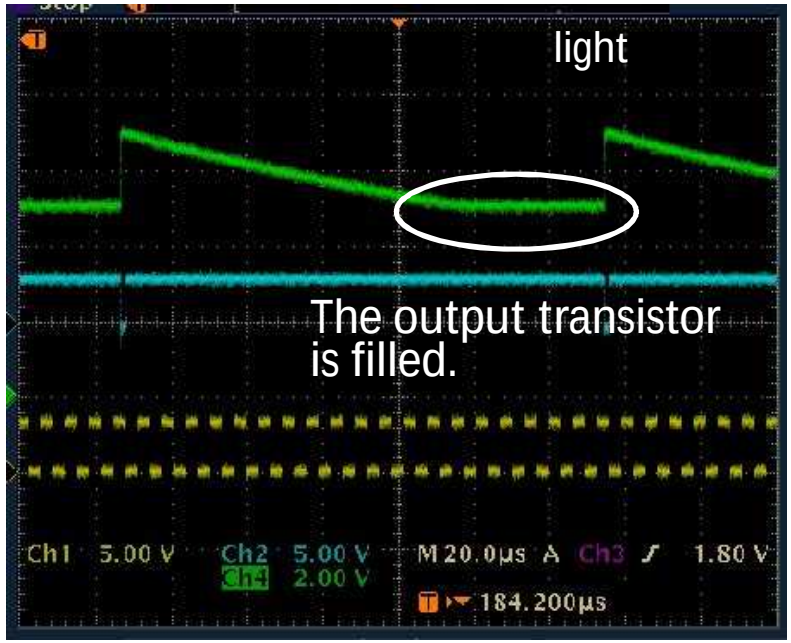




FPCCD output

- Check the output from FPCCD test-sample
  - Reset for each 20pixel, to check the CCD operation

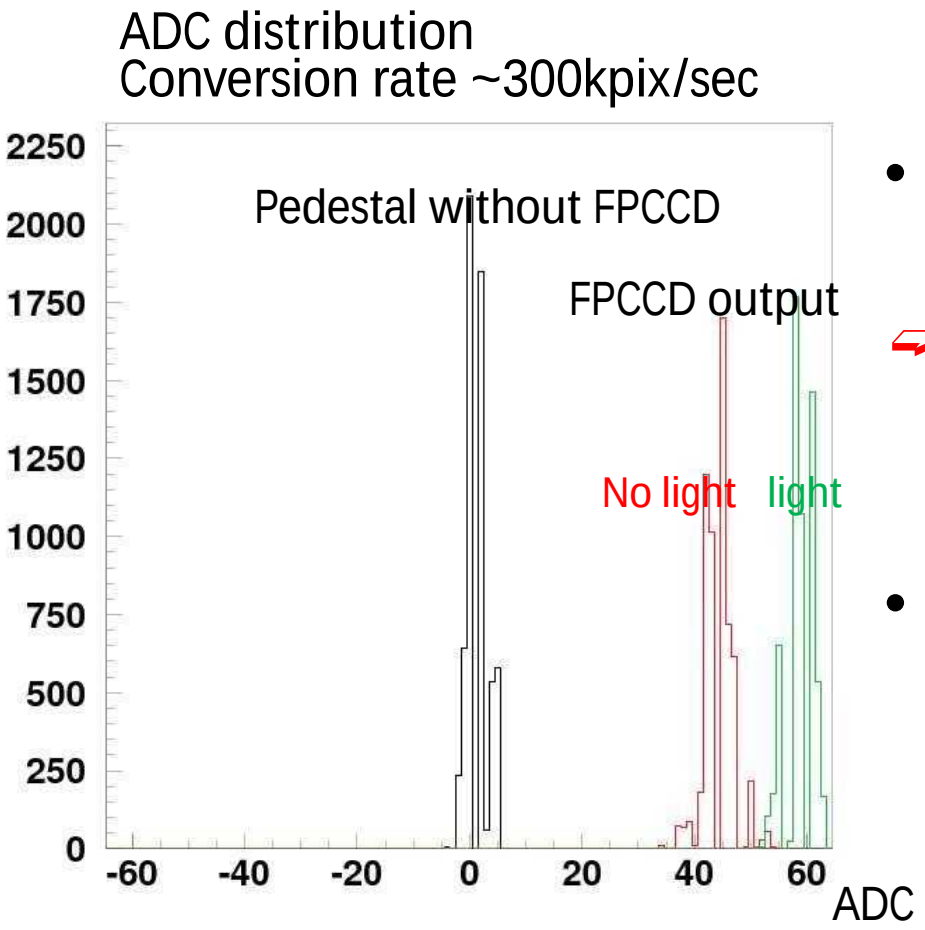




⇨ The output signal can be observed from the FPCCD .

Readout FPCCD

- The FPCCD test-sample was readout by the prototype ASIC



- The FPCCD test-sample was readout by the prototype ASIC

⇨ The ADC values change for the light intensity on the FPCCD.

- But, Dummy Channels that hardly reacts to light ware read.

⇨ It is necessary to readout pixels without Dummy channel.

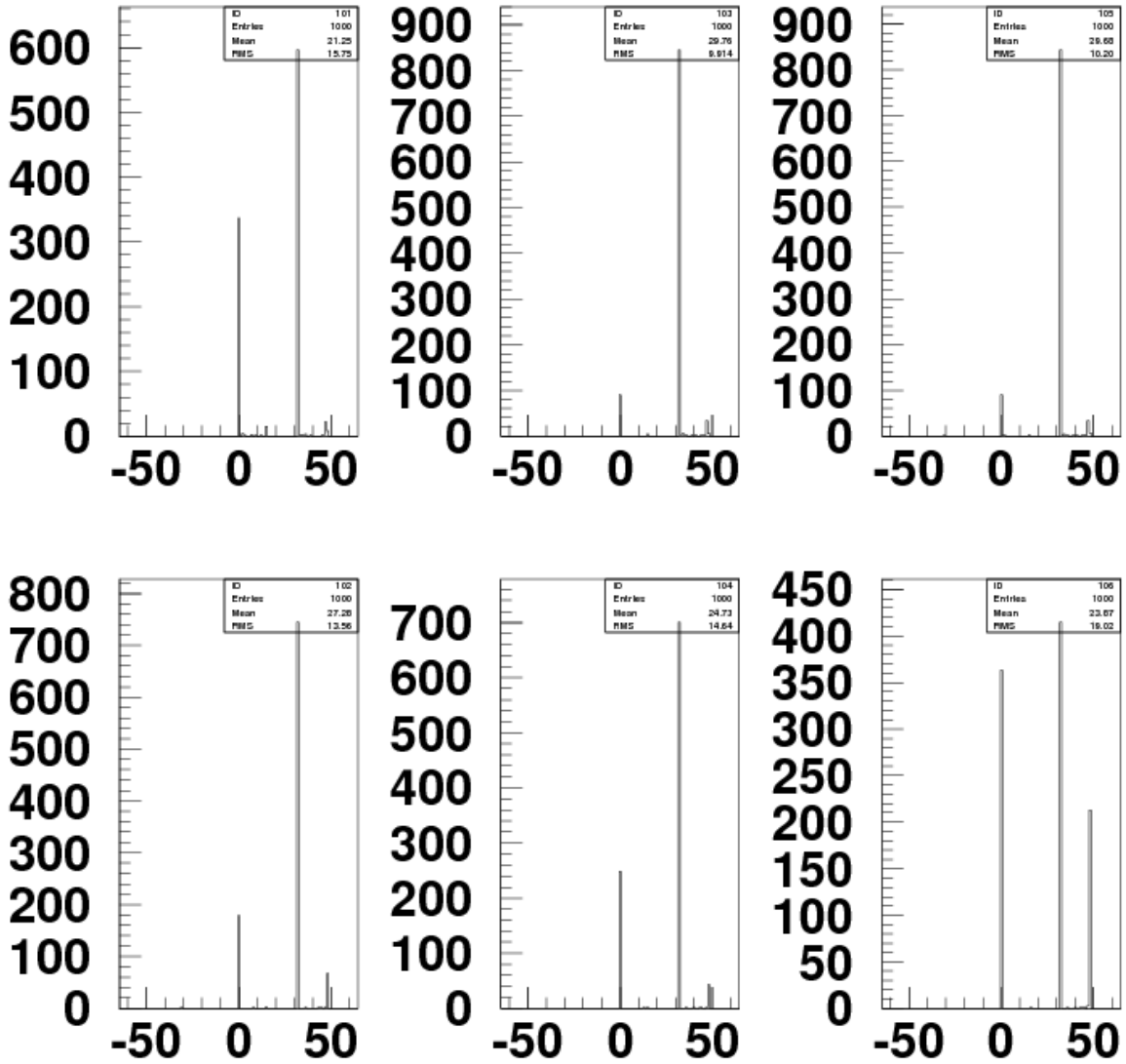
Summary

- We developed the readout ASIC for FPCCD
  - Test sample was delivered in March 2008
- The performance of the Test sample is checked
  - conversion rate：～1.5Mpix/sec
  - Noise level：～70e
  - ADC linearity：±80e
  - The ADC capacitor ratio is unbalanced by the floating capacitance at the switching circuit in the ADC → Improvement of the next test sample

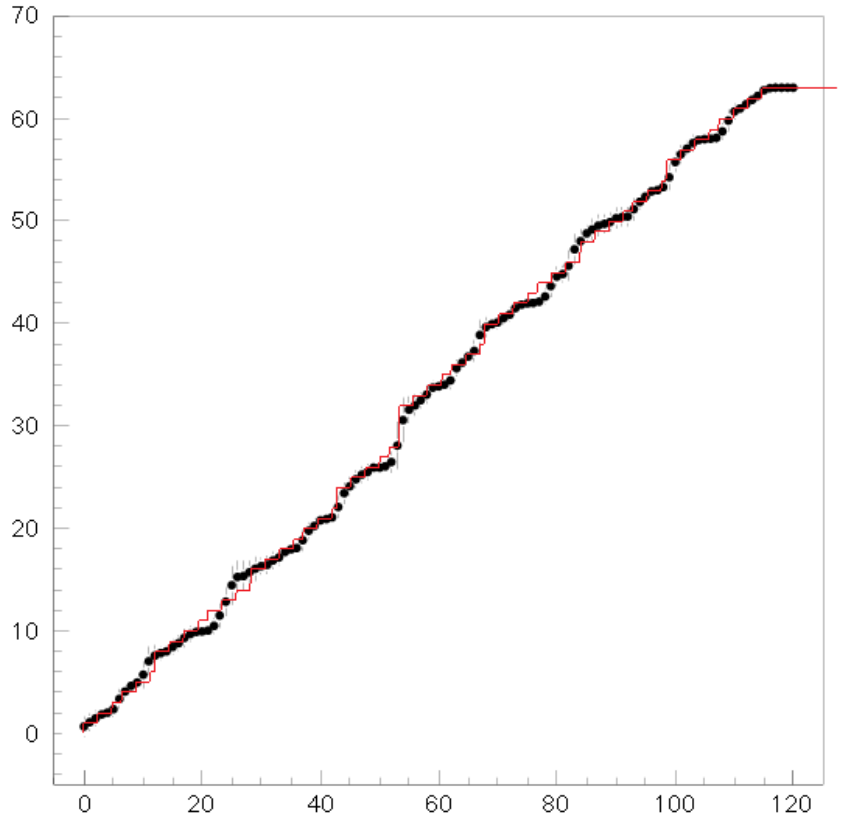
Next step

- **High speed readout**
- **FPCCD readout**
- **Noise level**

5MHz変換での周期性



ADCのコンデンサーの比



32 : 16 : 8 : 4 : 2 : 1

↓

34.5 : 19 : 9.5 : 5.5 : 3 : 1.5