Development of Pair-monitor

Y.Sato [A], H.Ikeda [B], K.Ito [A], A.Miyamoto [C], T.Nagamine [A],
R.Sasaki [A], Y.Takubo [A], T.Tauchi [C], H.Yamamoto [A]

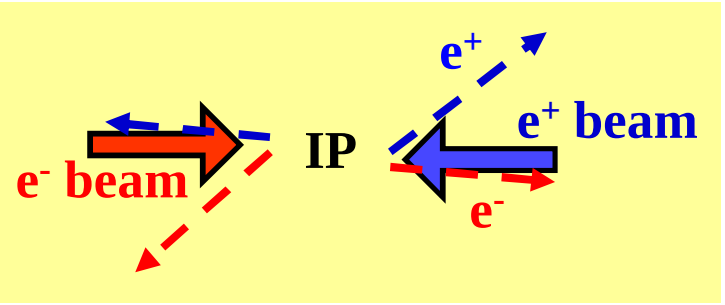
A : Tohoku University, B : JAXA, C : KEK

Outline

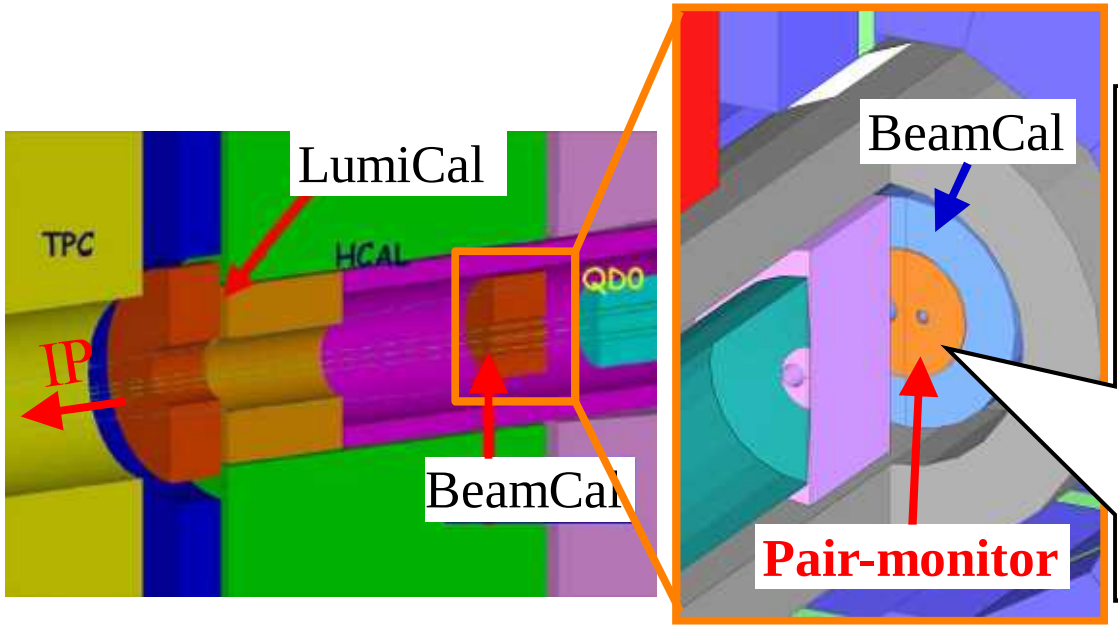
1. Introduction
   - Pair-monitor
2. Development of readout ASIC
   - Design and layout
   - Operation test
3. Development of Pair-monitor with SOI technology
4. Summary

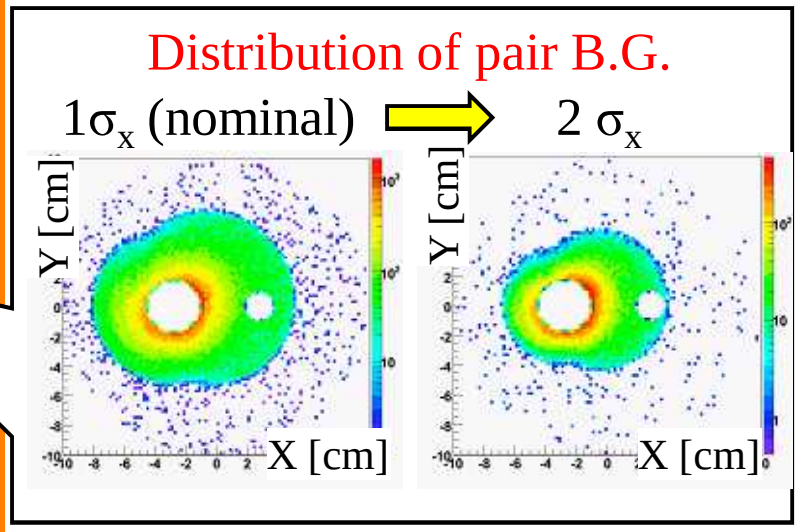
Pair-monitor

Pair-monitor is a silicon pixel detector to measure the beam profile at IP.



- The distribution of the pair B.G. is used.
  - The same charges with respect to the oncoming beam are scattered with large angle.
  - The scattered particles have information on beam shape.
- The location will be in front of the BeamCal.





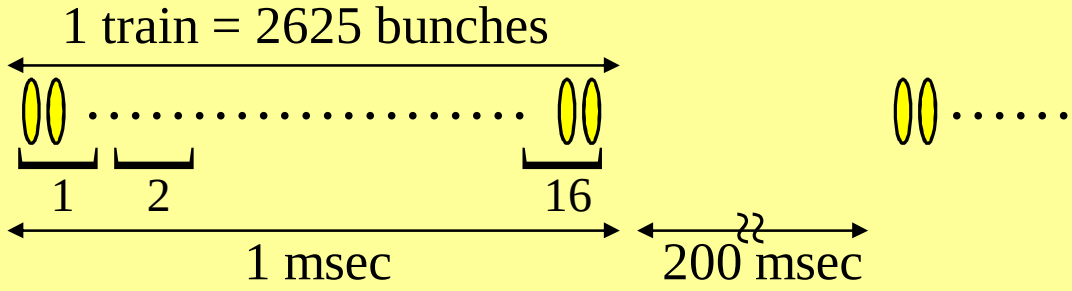
Development of the readout ASIC

As the first step, readout ASIC was developed.

Design concept of readout ASIC

- Pair-monitor measures the hit distribution of the pair B.G..
- Measurement is done for 16 parts in one train
  for the time-dependent measurement.
  - 16 hit counts are stored at each part.
  - Count rate : < 2.5 MHz / (400μm x 400μm)
  - Information of the energy deposit is not necessary.
- Data is read out during inter-train gaps. (~ 200 msec)

Beam structure



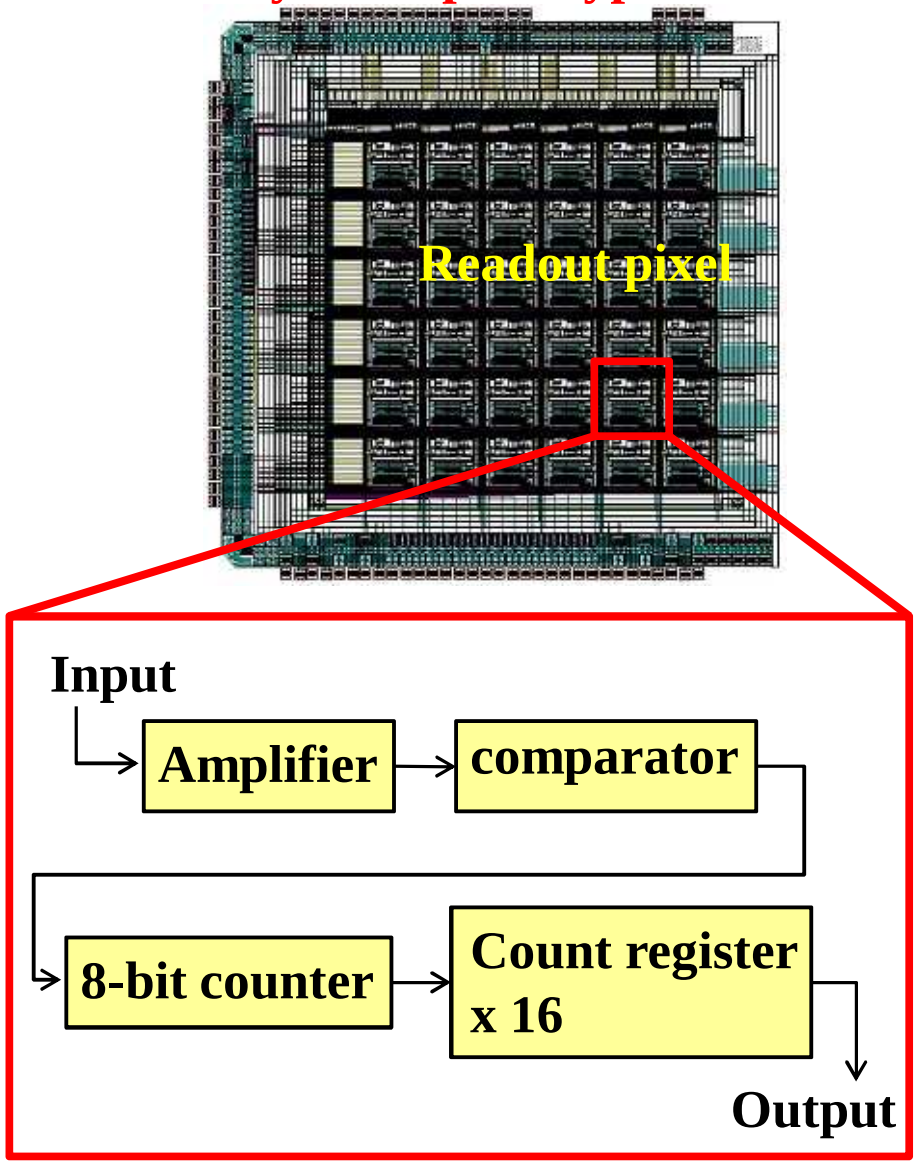
→ The prototype readout ASIC was designed to satisfy these concepts.

Design of readout ASIC

Design of readout ASIC

- 36 (6 x 6) readout pixels
  - Amplifier
  - comparator
  - 8-bit counter
    - ➢ to hit a number of hits
  - 16 count-registers
    - ➢ to store hit counts
- Shift register
  - ➢ to select a pixel from 36 pixels

Layout of prototype ASIC

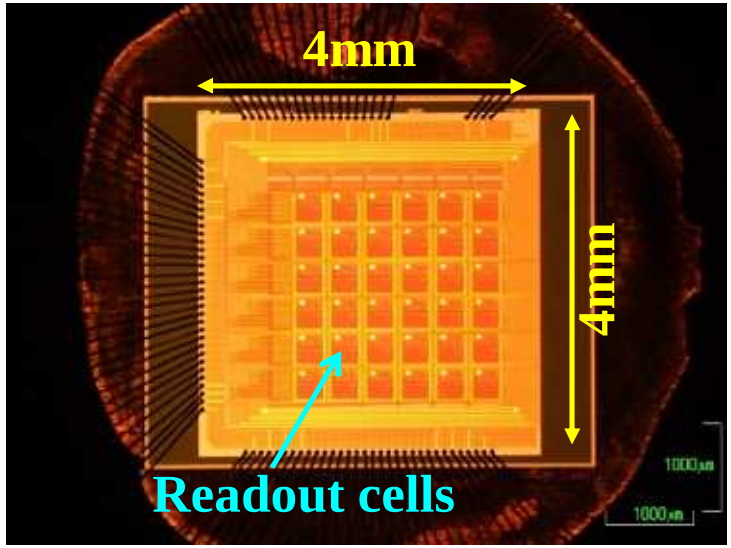


Prototype of Readout ASIC

The prototype of the readout ASIC was developed.

Prototype ASIC

- Production process : 0.25 μm TSMC
- Chip size : 4 x 4mm^2
- # of pixel : 36 (= 6x6)
- Pixel size : 400 x 400 μm^2
- Sensor will be bump-bonded to the ASIC.
- The chip was packaged in a PGA144.



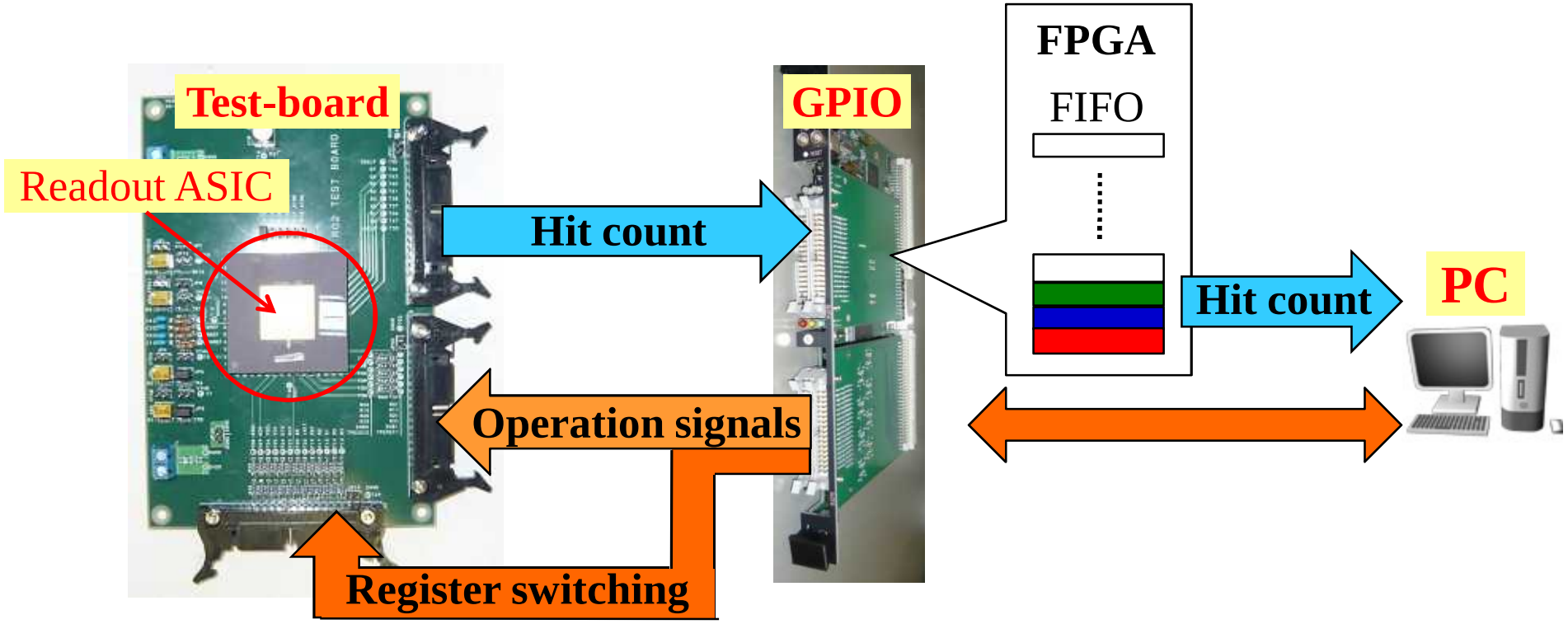
→ The production of the readout ASIC was done in Oct. 2008.

Test system

The operation test was performed.

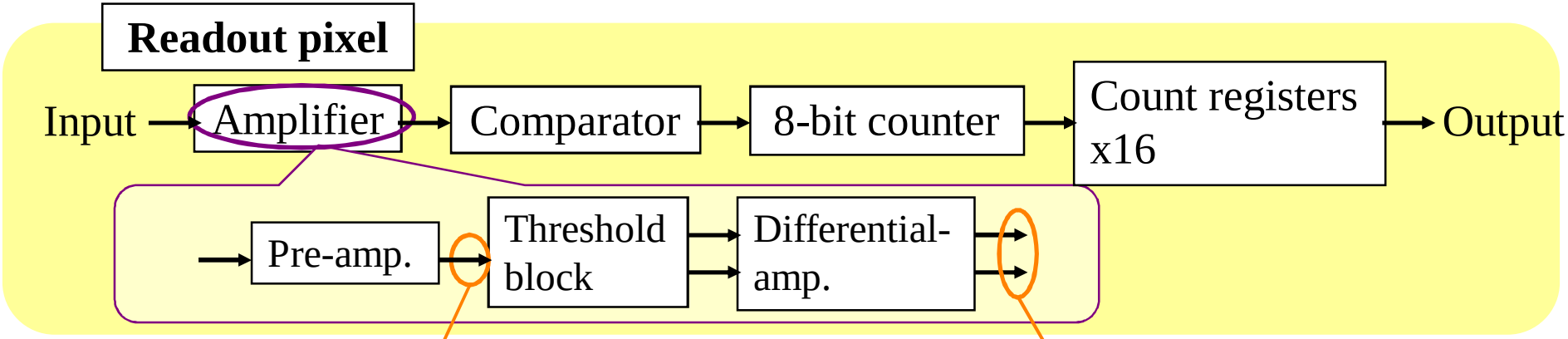
Test system

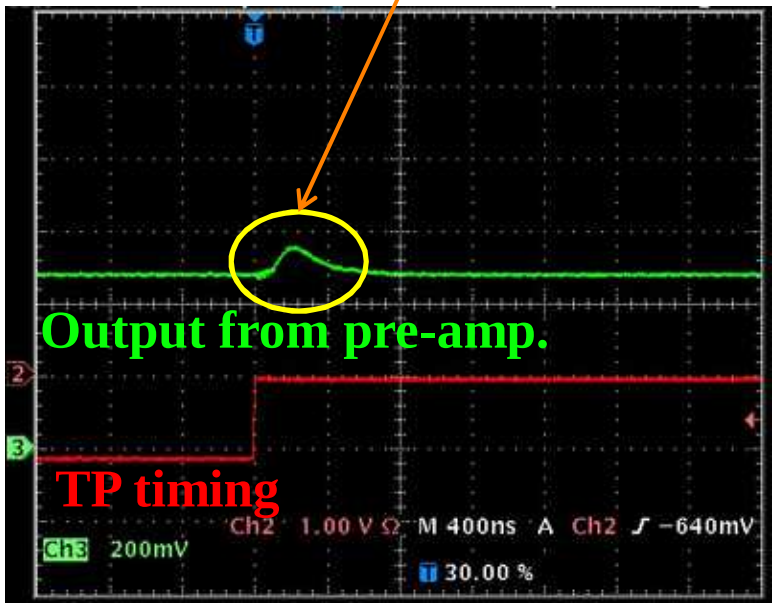
- GNV-250 module was used for the operation and readout .
  - KEK-VME 6U module
- The test-sequence by GPIO is controlled by a PC.

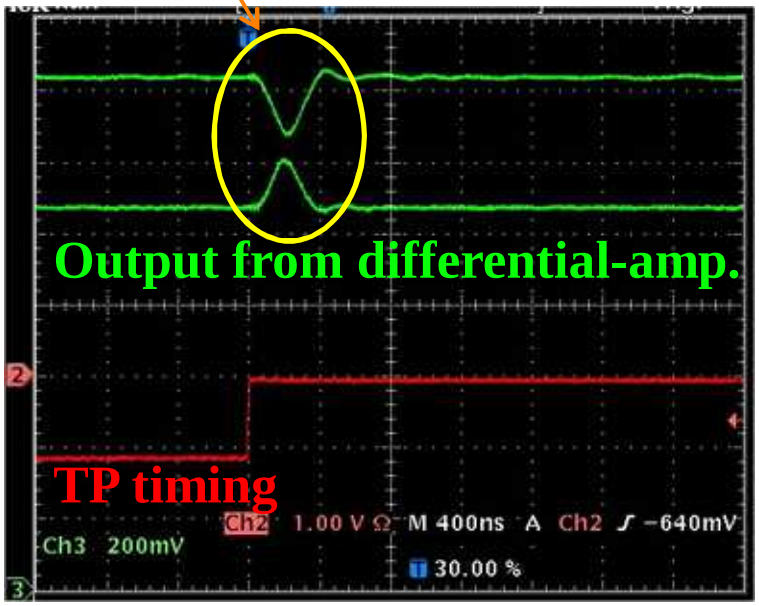


Response of amplifier block (Ⅰ)

The response of the amplifier block was checked.







→ The output signals were observed.

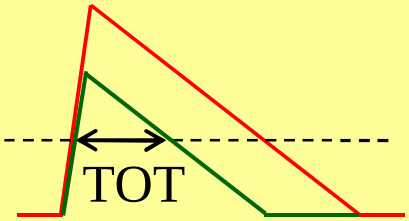
Response of amplifier block (Ⅱ)

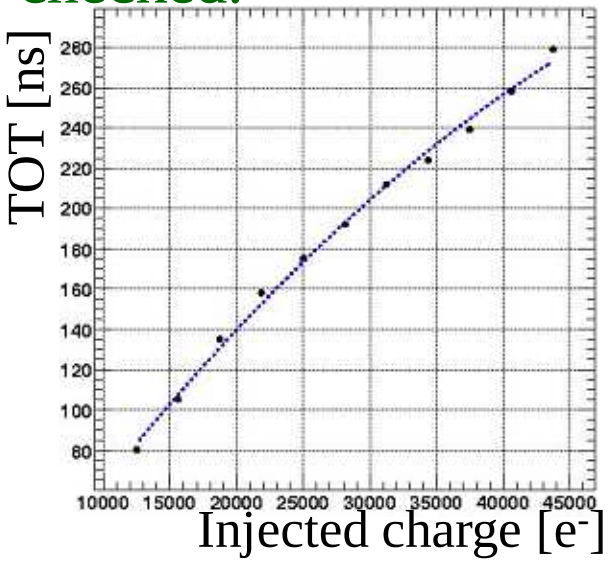
TOT (Time Over Threshold) characterization was checked.

Injected charge dependence

- TOT increases according to injected charge.

High charge
Low charge

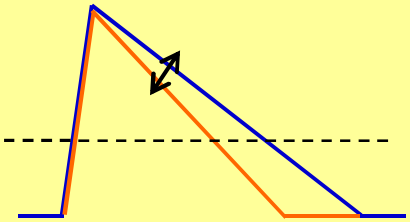


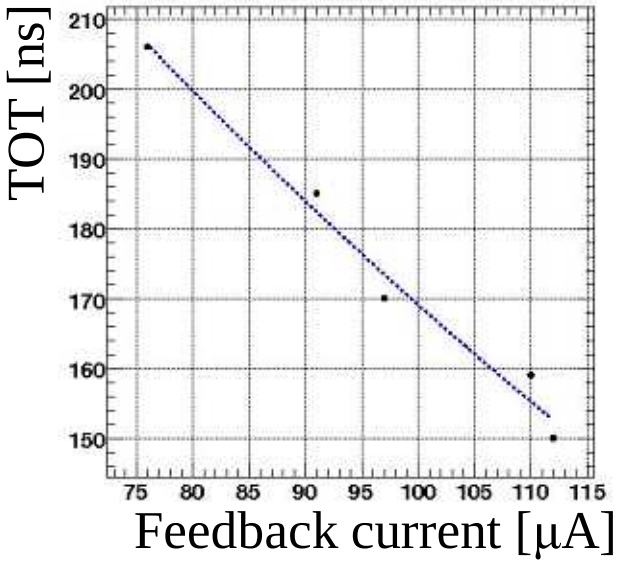


Feedback current dependence

- TOT decrease according to feedback current.

High feedback
Low feedback





→ The amplifier block works correctly.

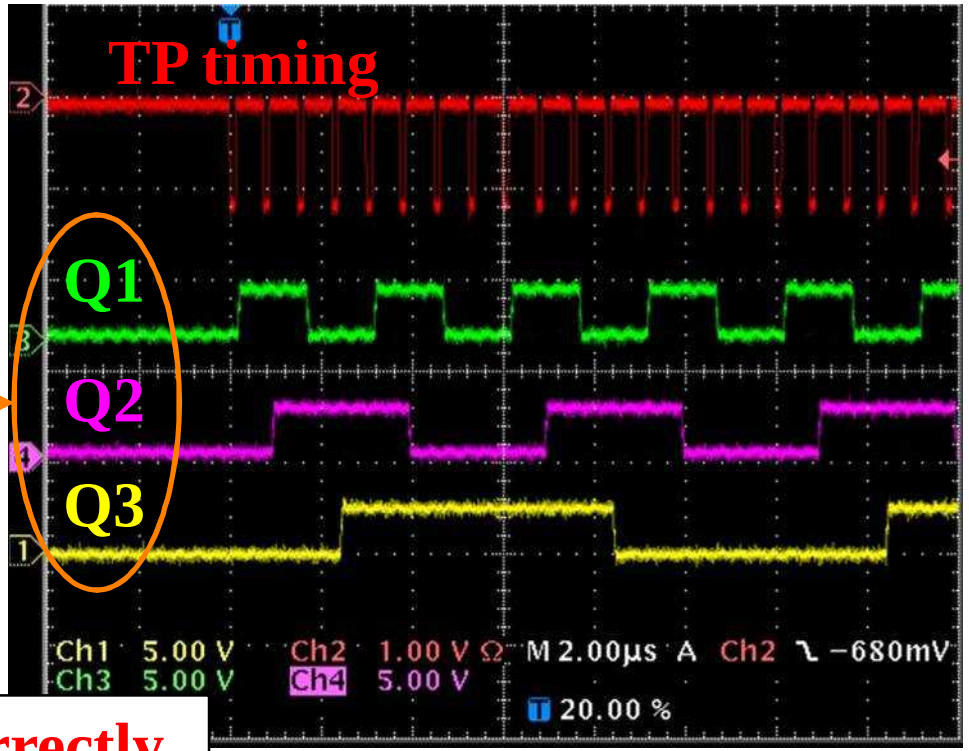
Response of counter block

The response of the counter block was checked.

Readout pixel

Input → Amplifier → Comparator → 8-bit counter → Count registers x16 → Output

Gray code is used.

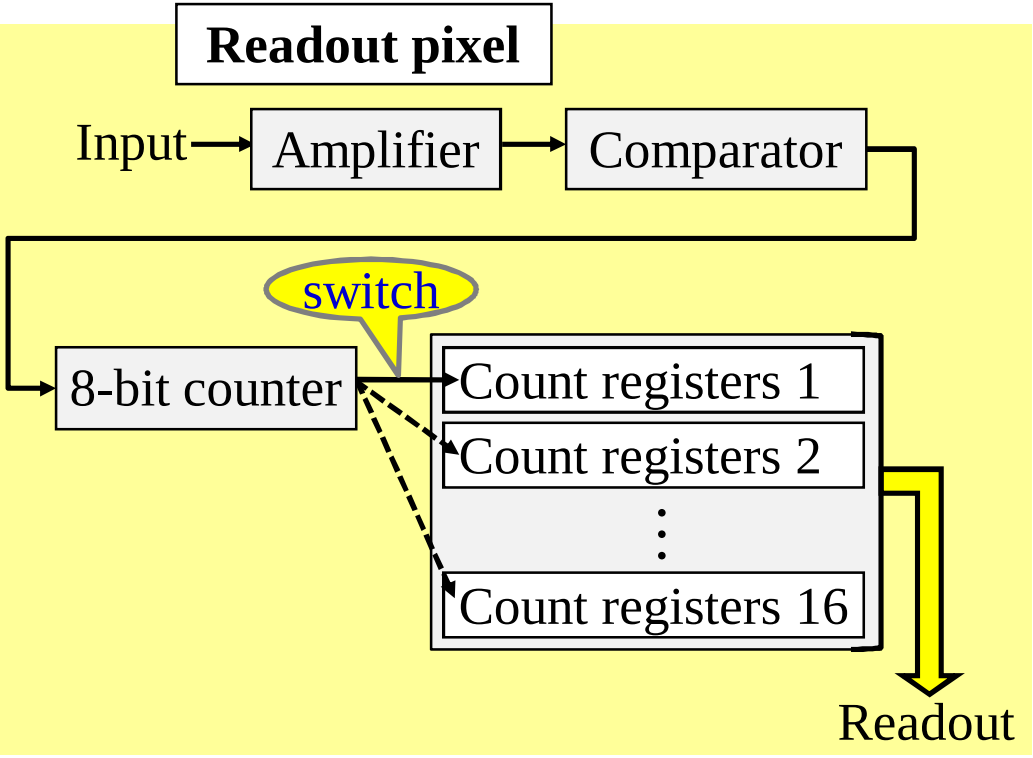


→ **The counter block works correctly.**

Readout of hit counts

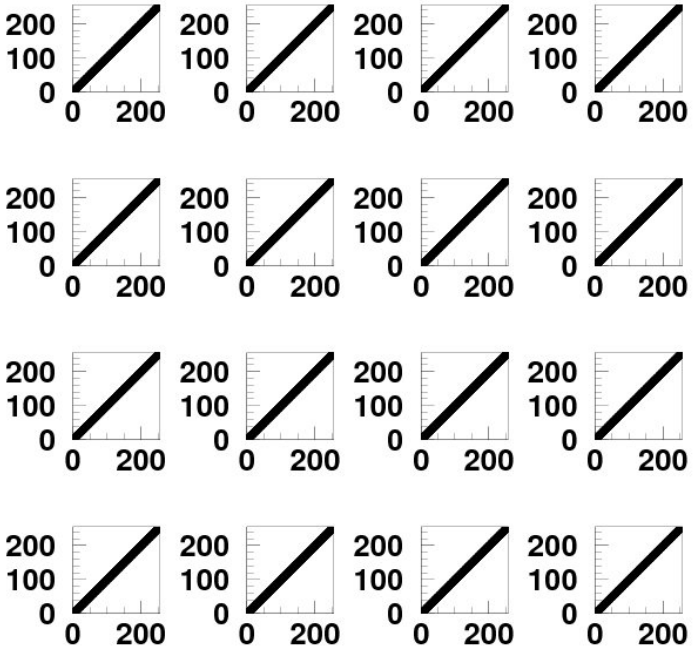
Readout of hit counts was checked.

- The hit count was stored at 4 MHz hit rate/ (400μm x 400μm) and read out from the count registers.



# of input TP

v.s. # of readout hit counts



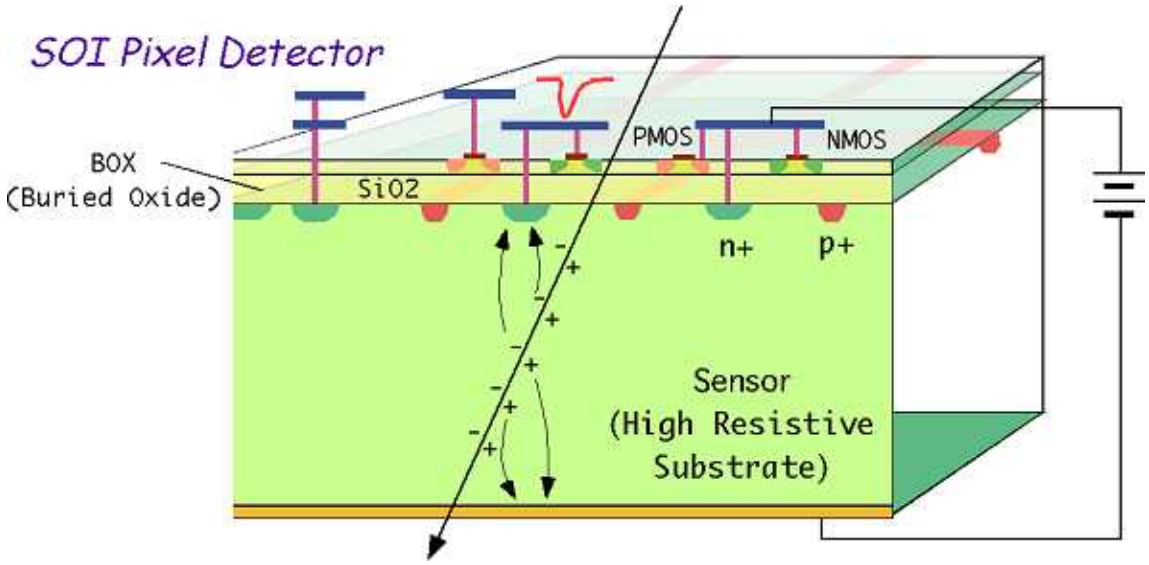
The readout ASIC was confirmed to work correctly as designed.

Pair-monitor with SOI technology

SOI (Silicon On Insulator) technology will be used
for development of the pair-monitor.

SOI pixel detector

- The sensor and readout electronics are integrated
  in the SOI substrate. (monolithic)
  - High speed
  - Lower power
  - Thin device
  - Low material



Development of the Pair-monitor with SOI technology was started,
participating in MPW (Multi Project Wafer) Run at KEK.

Prototype of SOI chip

For the next prototype, only the readout ASIC will be developed.

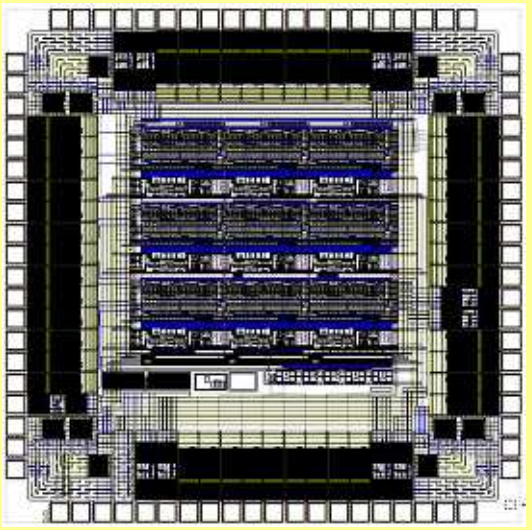
The layout of the readout ASIC was finalized.

Prototype ASIC

- Production process : FD - SOI CMOS 0.2 μm
- Chip size : 2.5 x 2.5 mm^2
- # of pixel : 9 (= 3 x 3)
- Design of the ASIC is modified a little.
  - Pole-zero cancellation
  - One comparator → Two comparators
  - TOT circuit → RC circuit

The operation test will be started in 2009.

Layout of readout ASIC



Summary

- Pair-monitor is the silicon pixel detector
  to measure the beam profile at IP.
- The prototype of the readout ASIC was developed.
  - The chip works correctly as designed.
- The next readout ASIC will be developed with SOI technology.
  - The layout was finalized.
  - The operation test will be started in 2009.