Development of Readout ASIC for Pair-monitor with SOI

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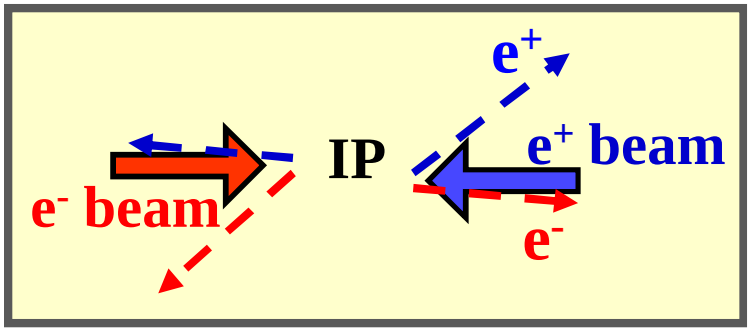
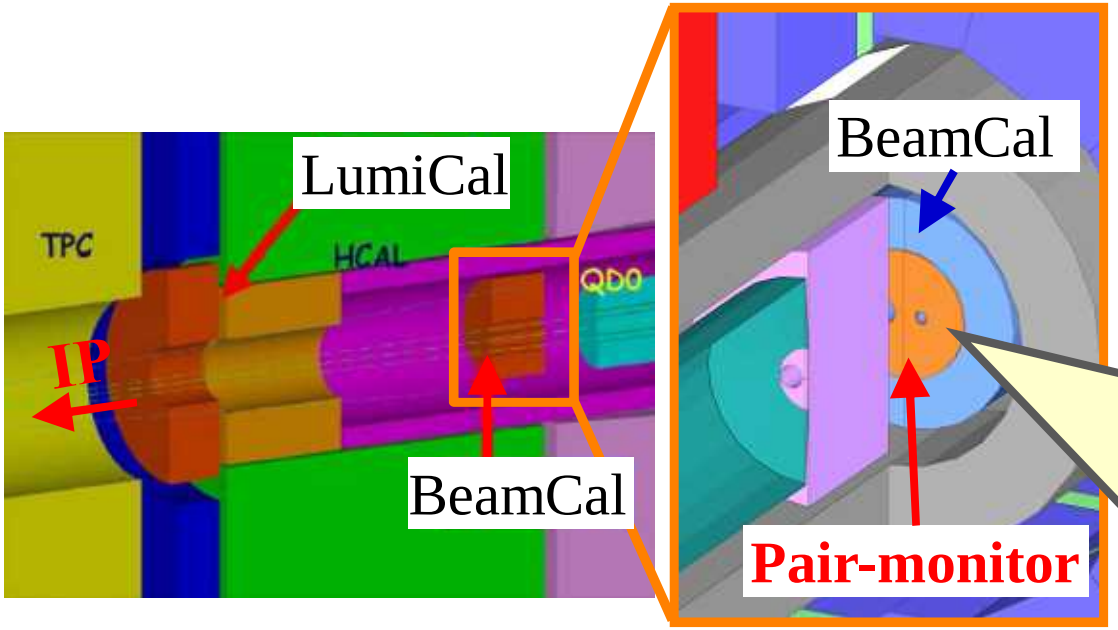
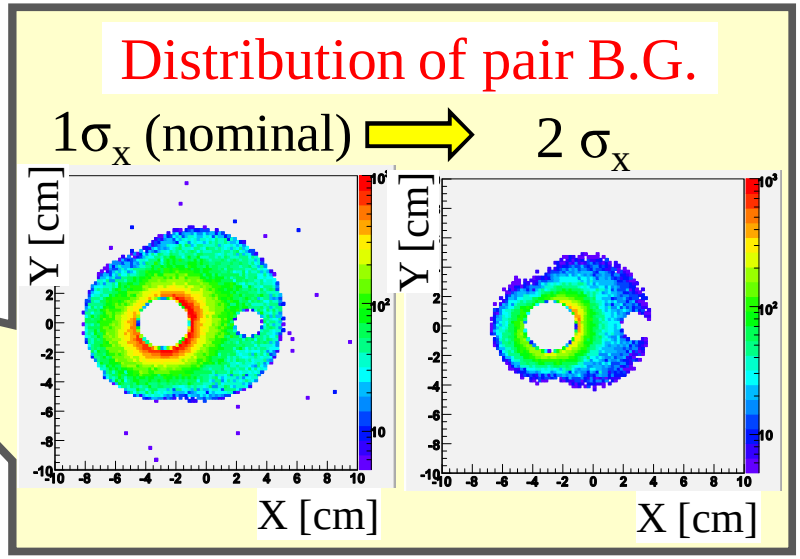
Pair-monitor

Pair-monitor is a silicon pixel detector to measure the beam profile at IP.



- The distribution of the pair B.G. is used.
  - The same charges with respect to the oncoming beam are scattered with large angle.
  - The scattered particles have information on beam shape.
- The location will be in front of the BeamCal.

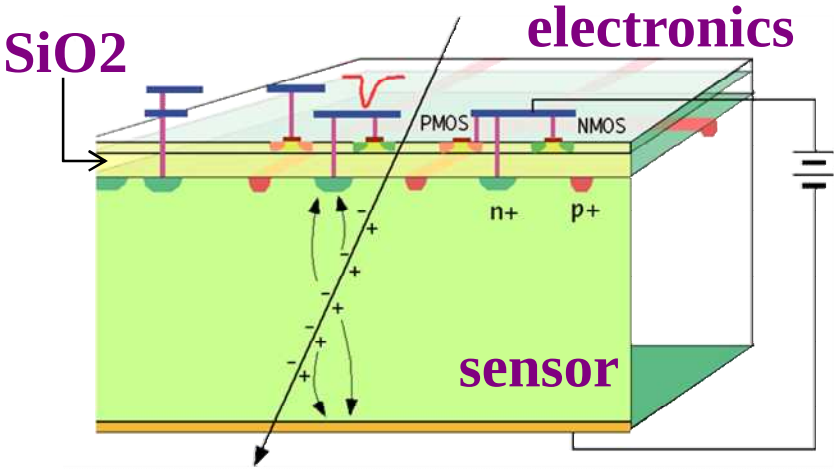




Development of Pair-monitor with SOI technology

SOI (Silicon On Insulator) pixel detector

- The sensor and electronics are integrated in the SOI substrate.
  - ➢ Monolithic device, high speed, low power, thin device, low material



Pair-monitor
- Pixel size : 400 x 400 μm^2
- Radius : 10 cm
- Total number of pixel : **~200,000**

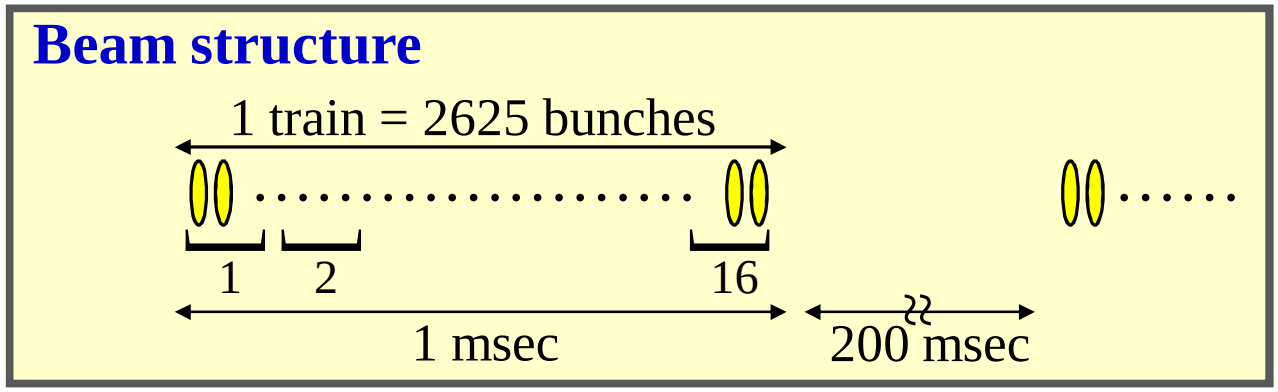
→ Monolithic device allows the elimination of bump-bonding process.

We started to develop the pair-monitor with SOI technology.
As the first step, only the readout electronics was produced.

Development of the readout ASIC

Design concept of readout ASIC

- Pair-monitor measures the hit distribution of the pair B.G..
- Measurement is done for 16 parts in one train
  for the time-dependent measurement.
  - 16 hit counts are stored at each part.
  - Count rate : < 2.5 MHz / (400μm x 400μm)
  - Information of the energy deposit is not necessary.
- Data is read out during inter-train gaps. (~ 200 msec)



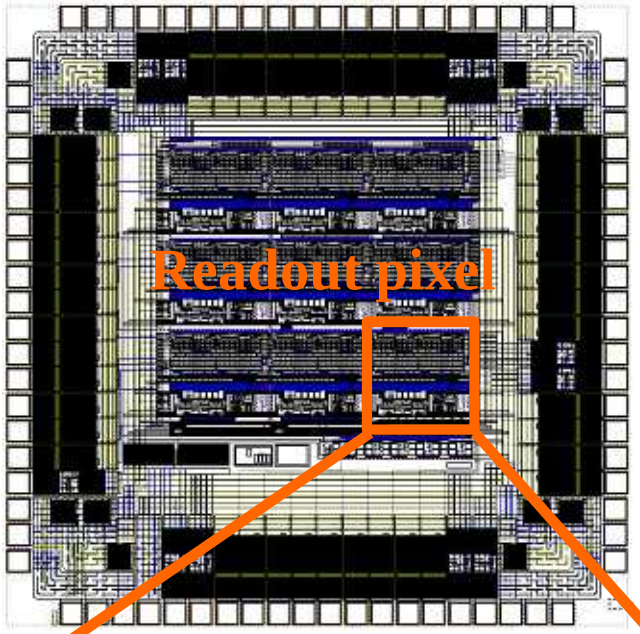
The prototype readout ASIC was designed to satisfy these concepts.

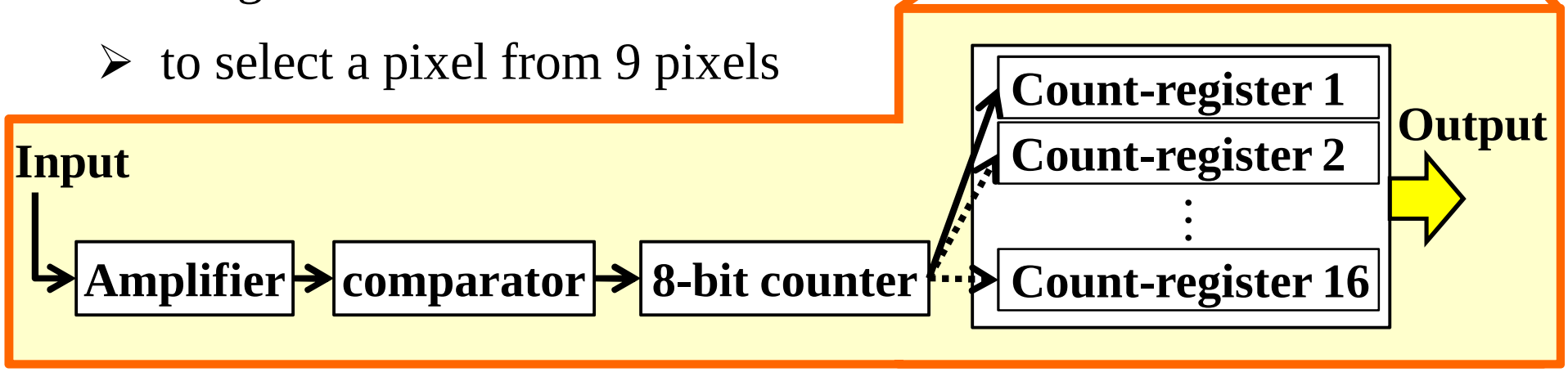
Design of readout ASIC

Design of readout ASIC

- 9 (3x3) readout pixels
  - Amplifier
  - comparator
  - 8-bit counter
    - to count the number of hits
  - 16 count-registers
    - to store hit counts
- Shift-register
  - to select a pixel from 9 pixels

Layout of prototype ASIC





Prototype of SOI chip

The prototype of the SOI chip was developed.

Prototype chip

- FD-SOI CMOS 0.2 μm process
- Chip size : 2.5 x 2.5mm^2
- # of pixel : 9 (= 3x3)
- Only the readout ASIC was fabricated.
- Package : QFP80

Packaged ASIC

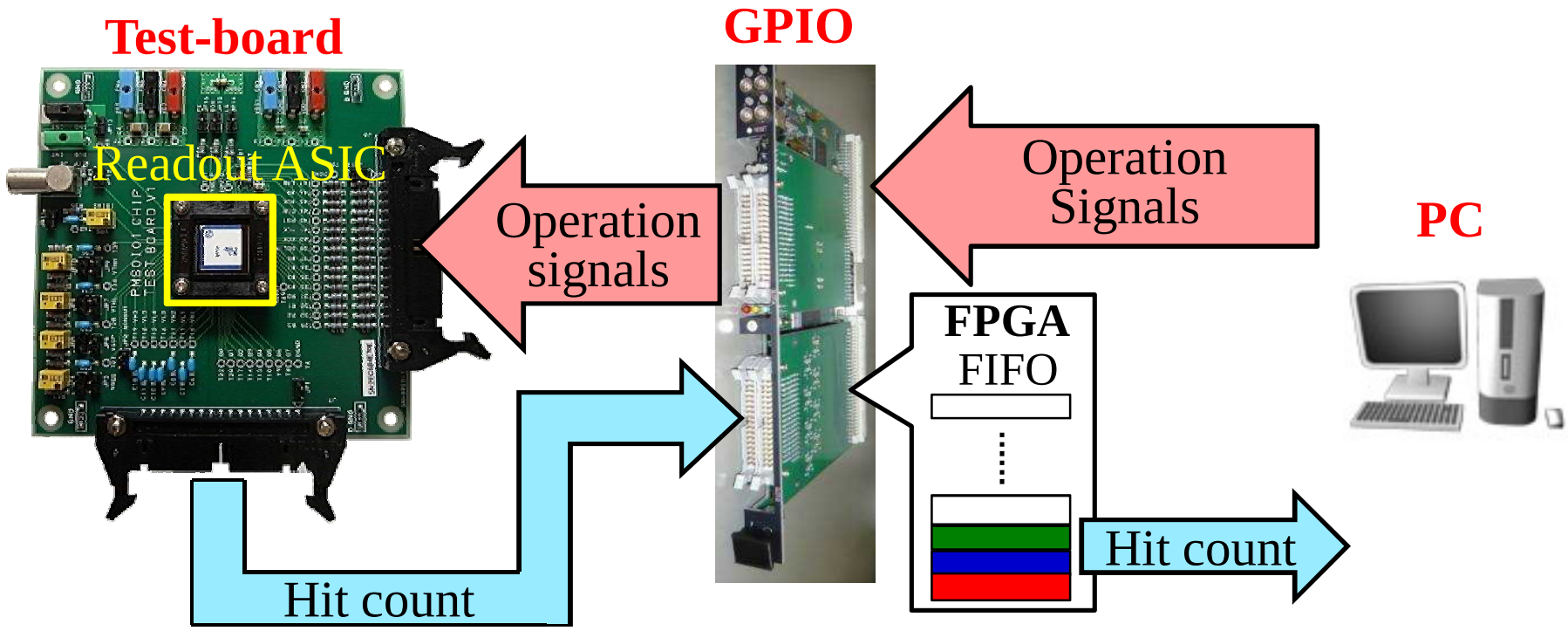
The production of the readout ASIC was done in Aug. 2009.

Test system

The operation test was performed.

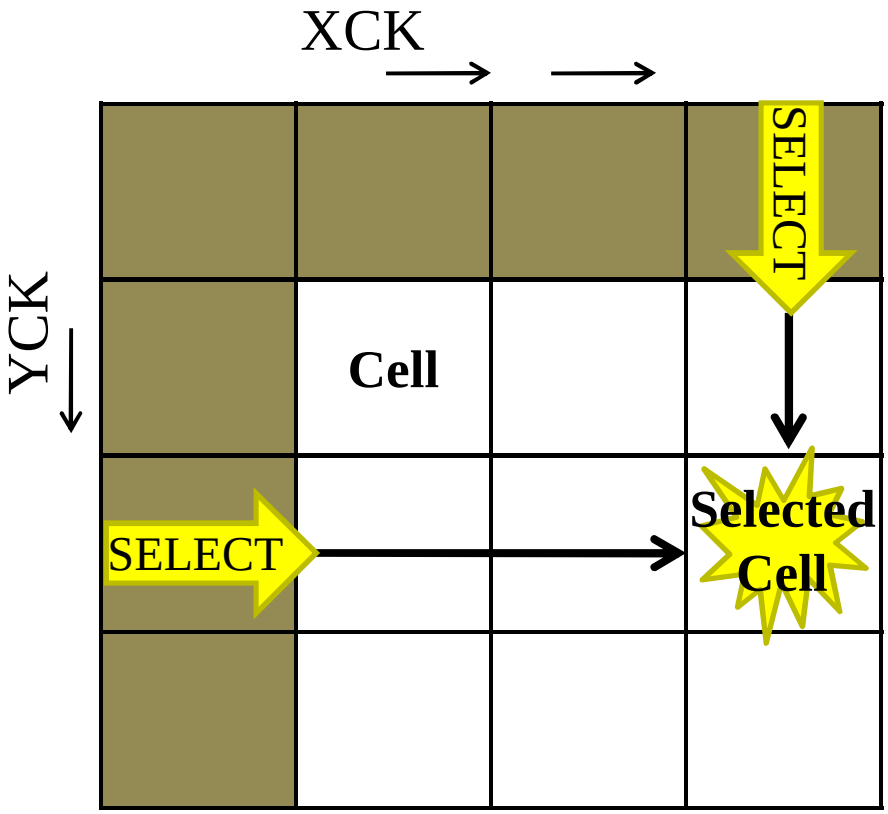
Test system

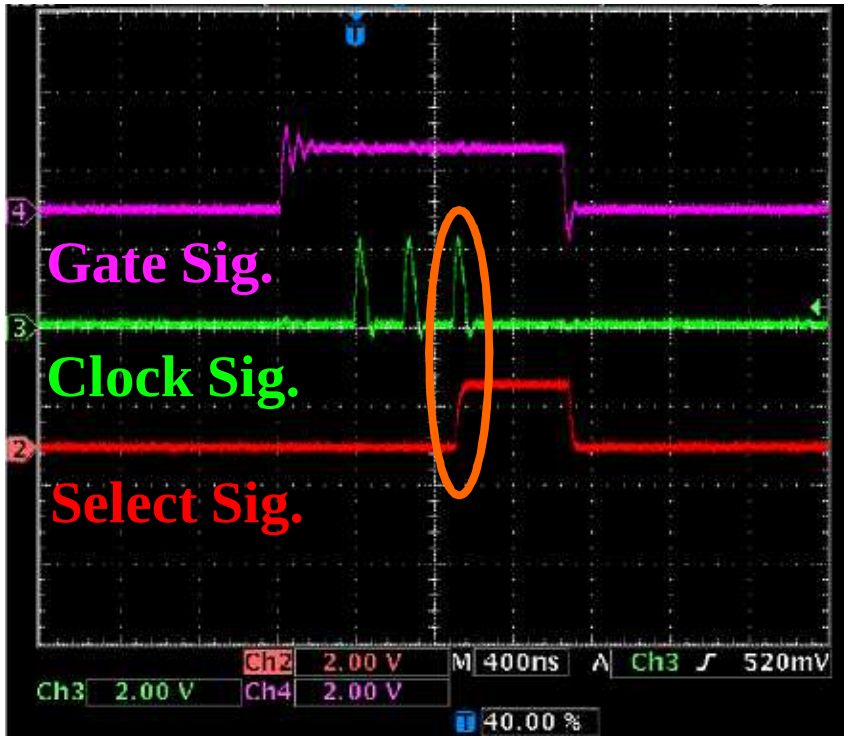
- GNV-250 module was used for the operation and readout .
  - KEK-VME 6U module
- The test-sequence by GPIO is controlled by a PC.



Response of shift-register

The response of the shift-register was checked.

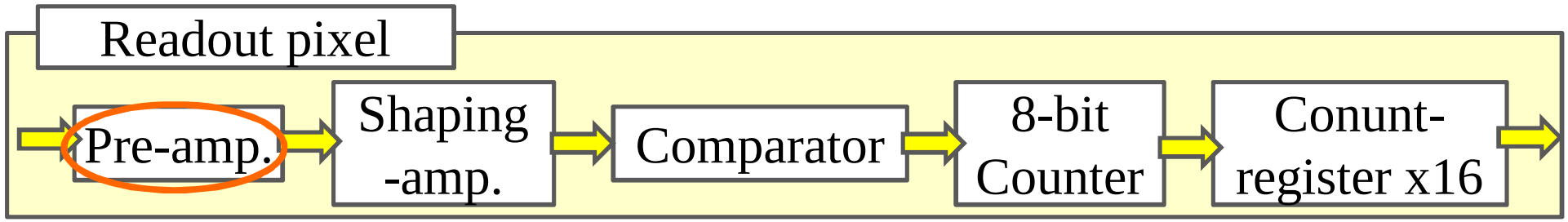




- The select signal rose at the third clock signal.

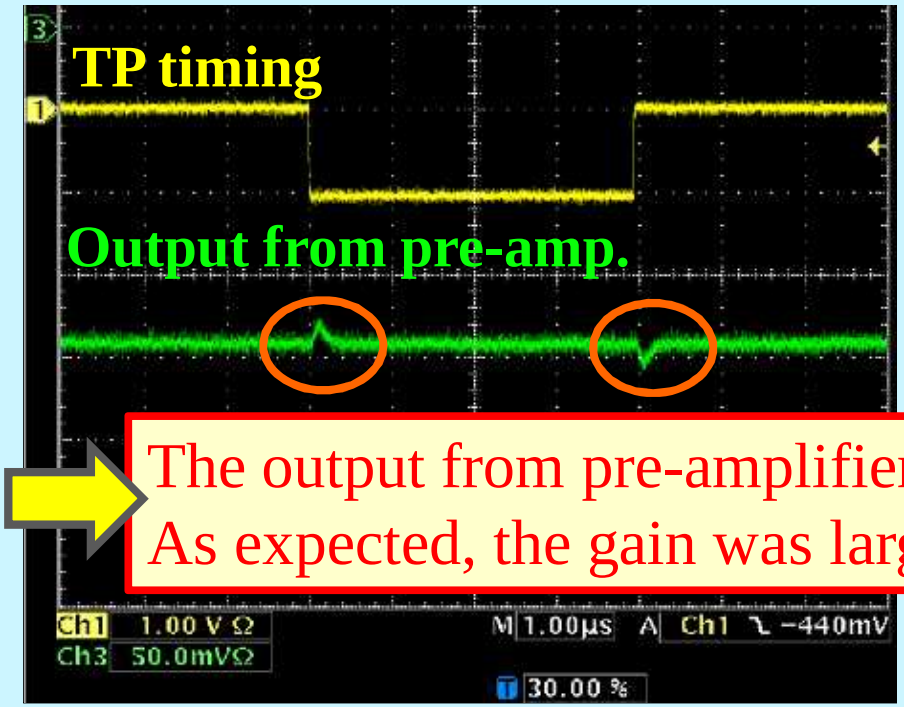
The shift-register works correctly.

Response of pre-amplifier

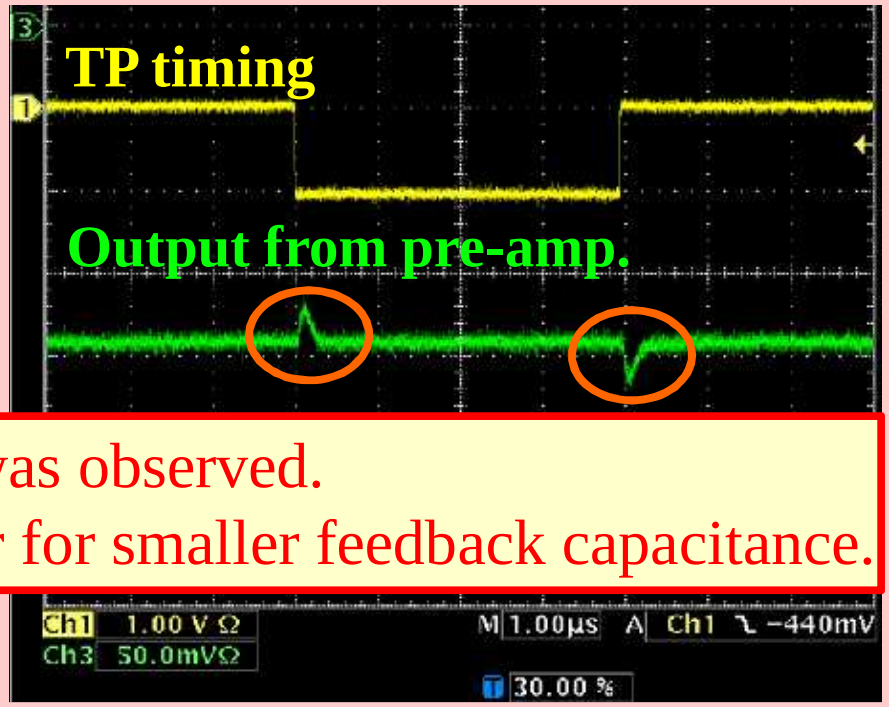


The output of the pre-amplifier was checked.

Feedback capacitance : 0.1 [pF]

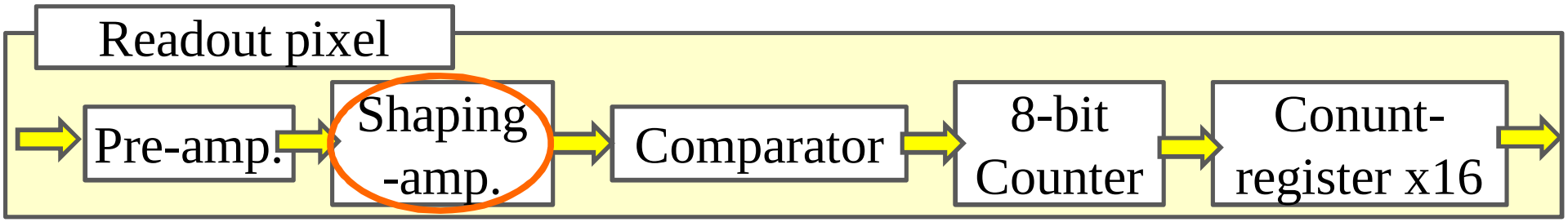


Feedback capacitance : 0.05 [pF]



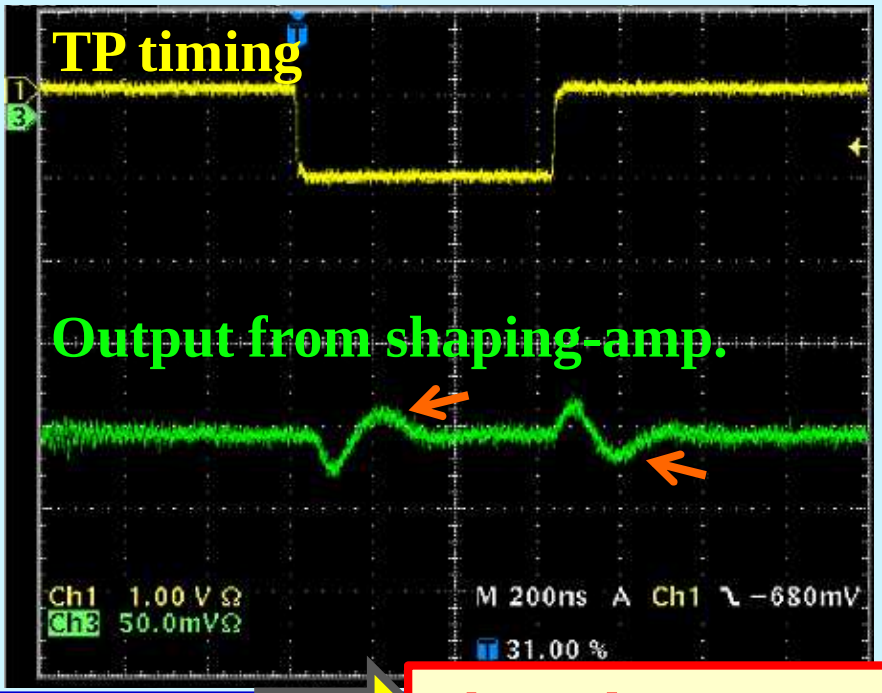
The output from pre-amplifier was observed.
As expected, the gain was larger for smaller feedback capacitance.

Response of shaping-amplifier

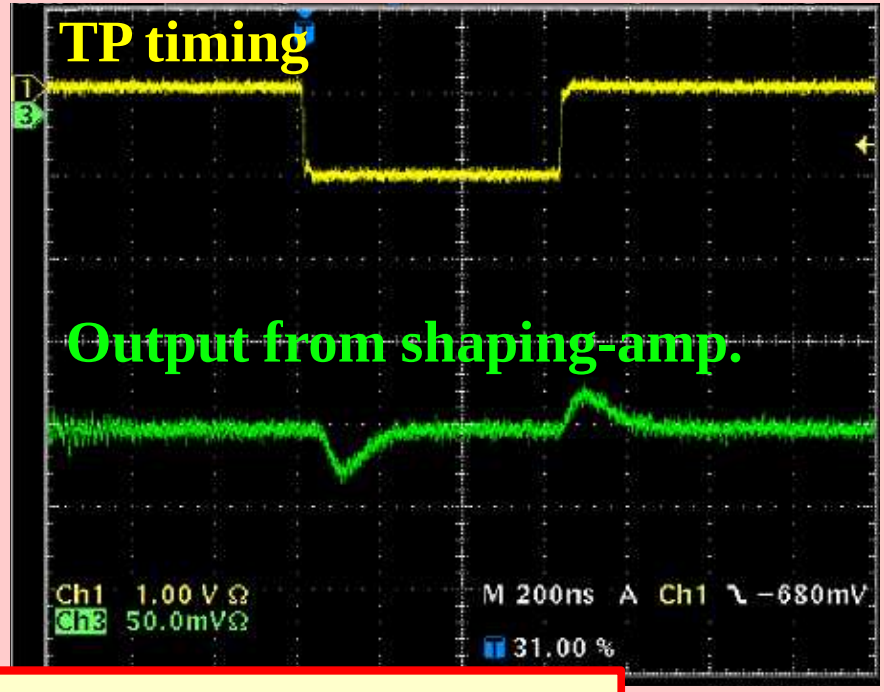


The output of the shaping-amplifier was checked.

Pole-zero cancellation OFF

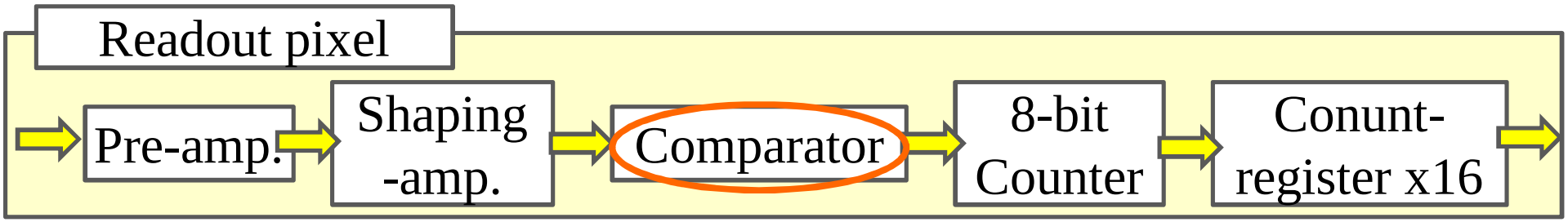


Pole-zero cancellation ON



The pole-zero cancellation works correctly.

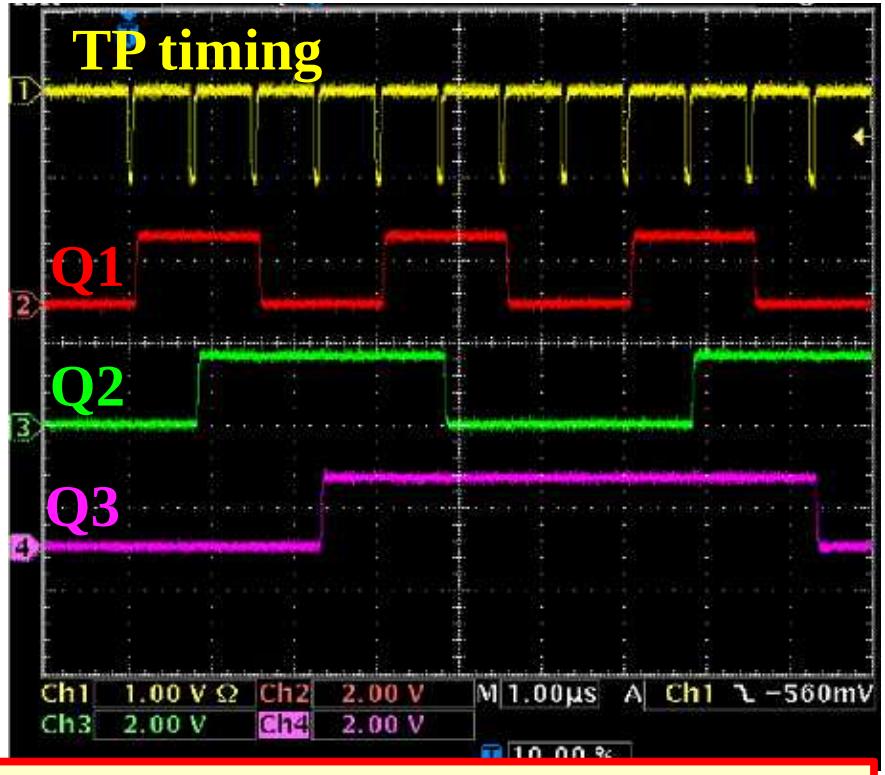
Response of counter block



The response of the 8-bit counter was checked.

- Gray code is used.
  - ➢ two successive values differ in only one bit.

Binary-code	Gray-code
000	000
001	001
010	011
011	010
100	110

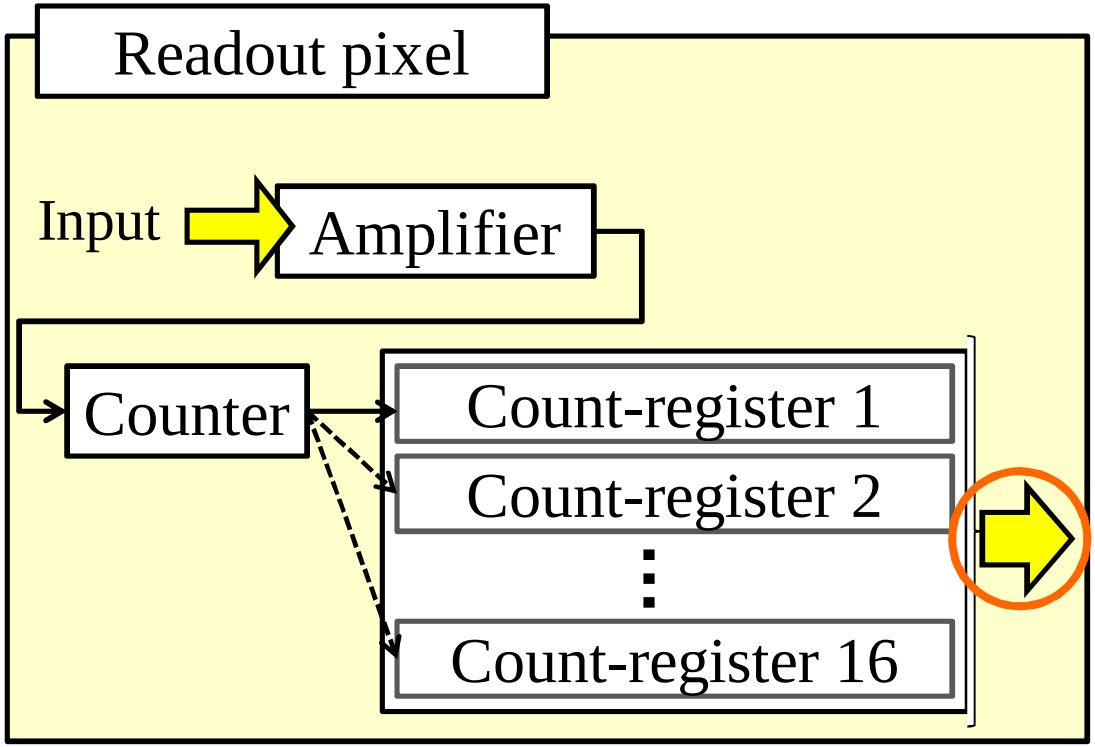


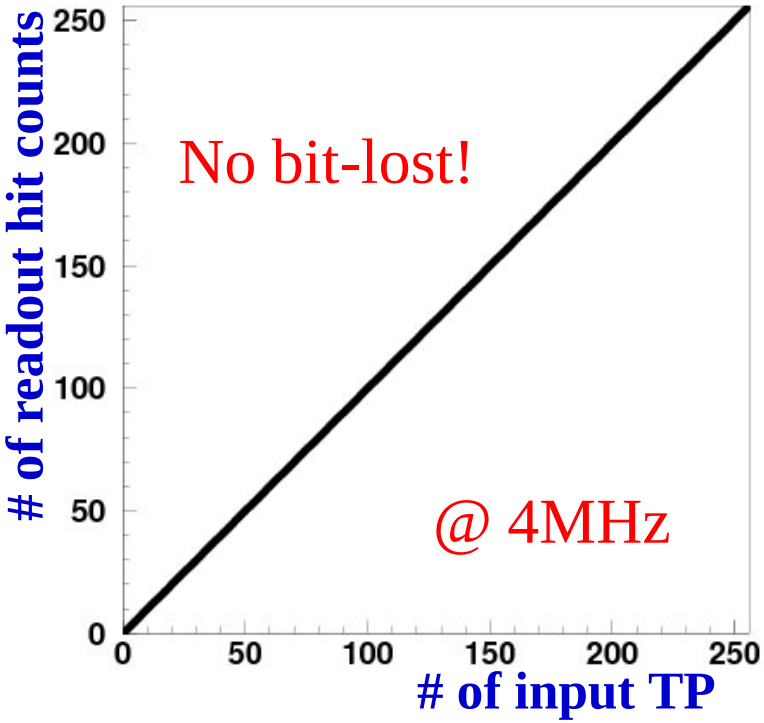
The counter block works correctly.

Readout of hit counts

Readout of hit counts was checked.

- The hit count was stored at 4 MHz hit rate/ (400μm x 400μm) and read out from the count registers.



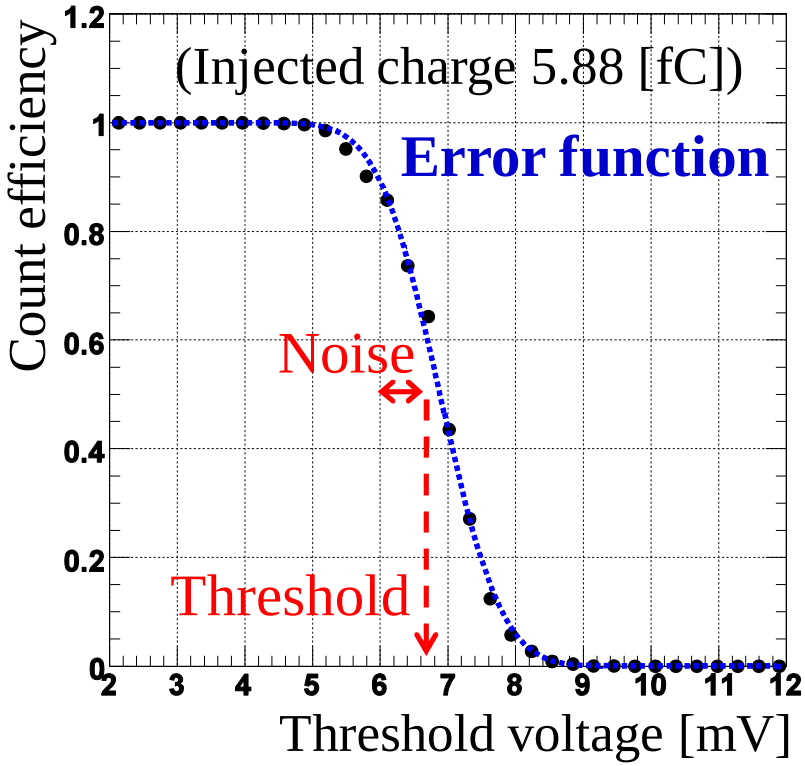


The correct hit counts were read out from count-register.

Noise characteristic (1)

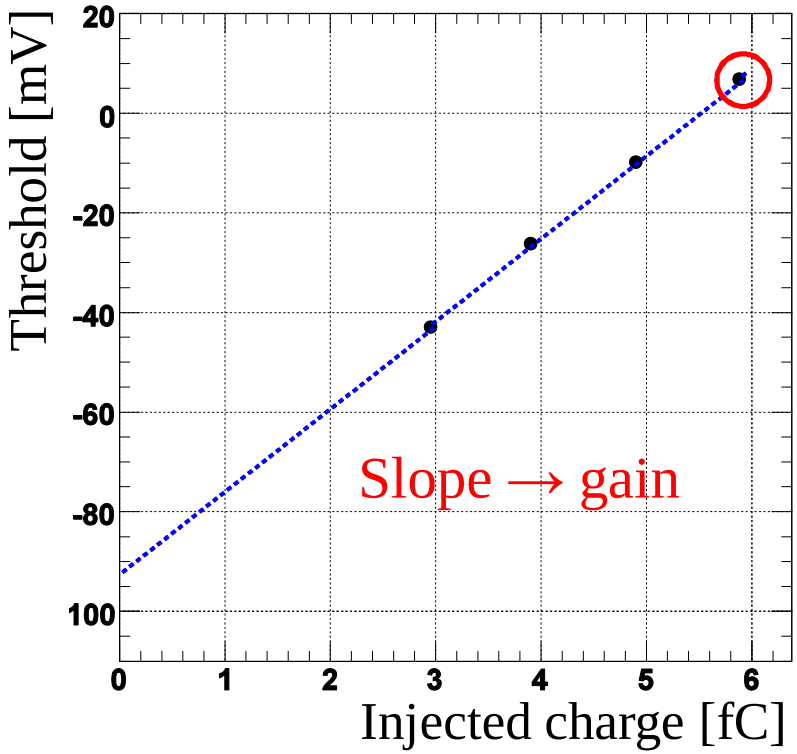
Threshold scan was performed.

- Fit to error function (S-curve)



- Threshold : 6.886 ± 0.009 [mV]
- Noise : 0.7152 ± 0.0128 [mV]

The gain was estimated to convert the noise into equivalent noise electrons.



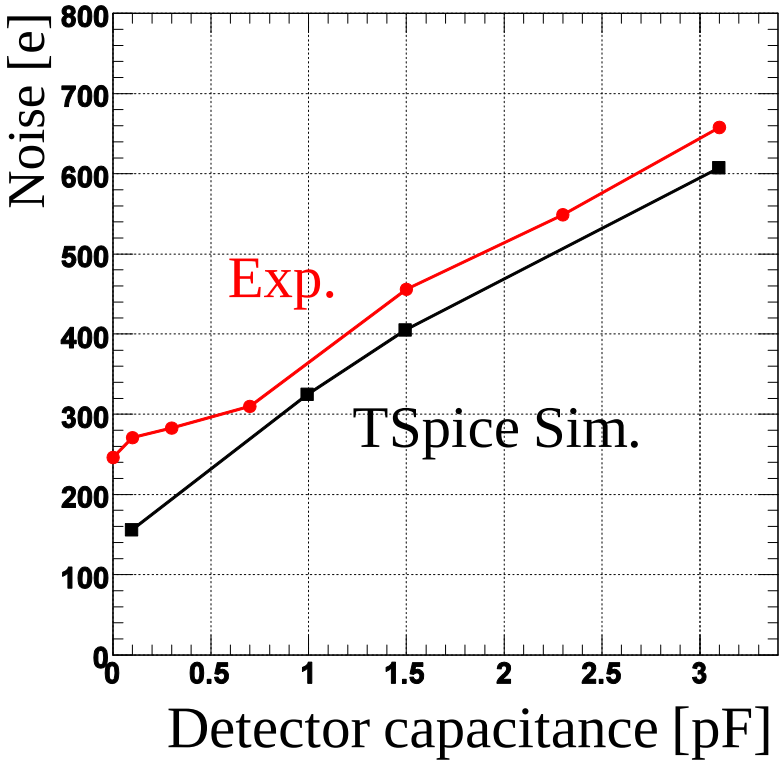
- Gain : 16.94 [mV/fC]

Noise : ~260 electrons

Noise characteristic (2)

The noise level was checked as a function of the detector capacitance.

- Each cell have different detector capacitance.



→ The noise level is 250 ~ 700 electrons.

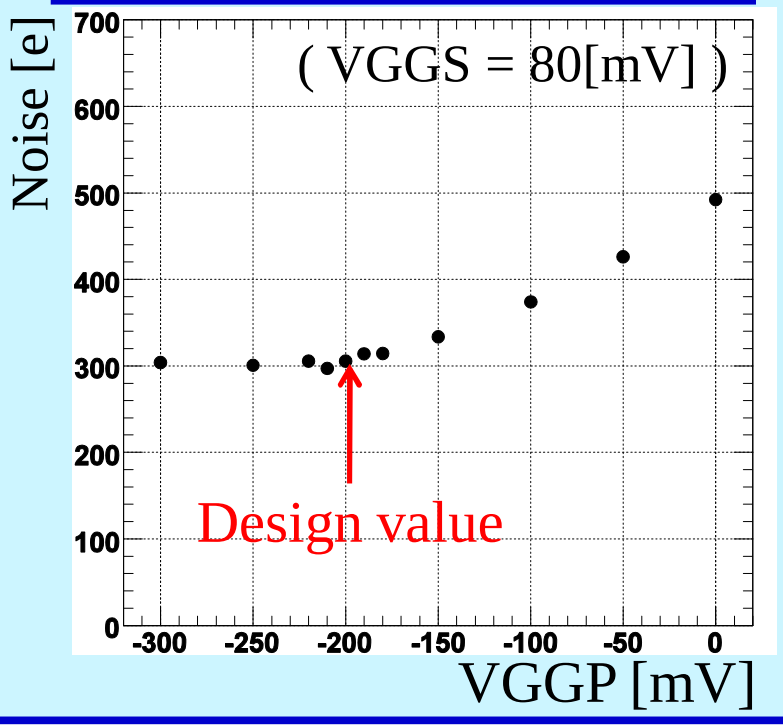
Noise is much smaller than typical signal level (~20,000 [e])

Stability of noise

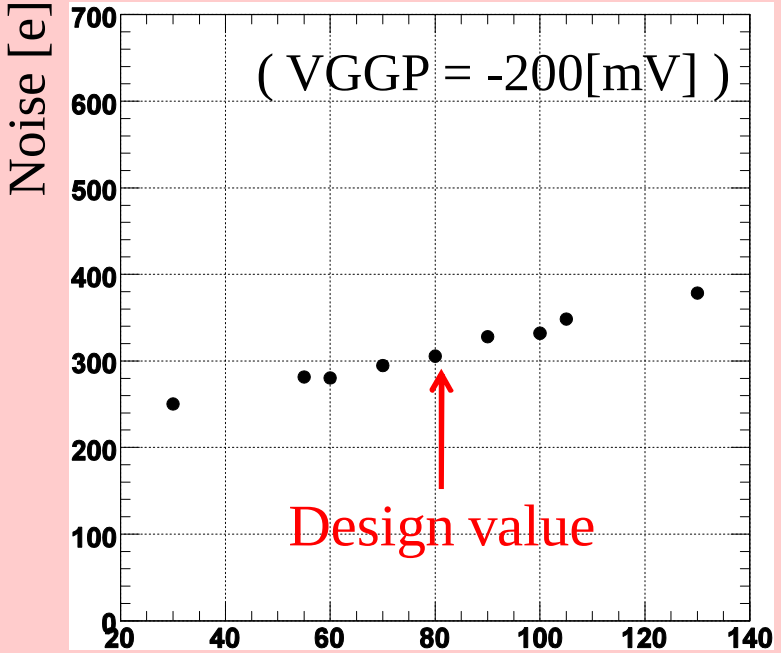
The stability of the noise was checked.

- The noise was evaluated in adjusting the time constant of amplifier circuits.

Time constant of pre-amp. (VGGP)



Time constant of shaping-amp. (VGGS)



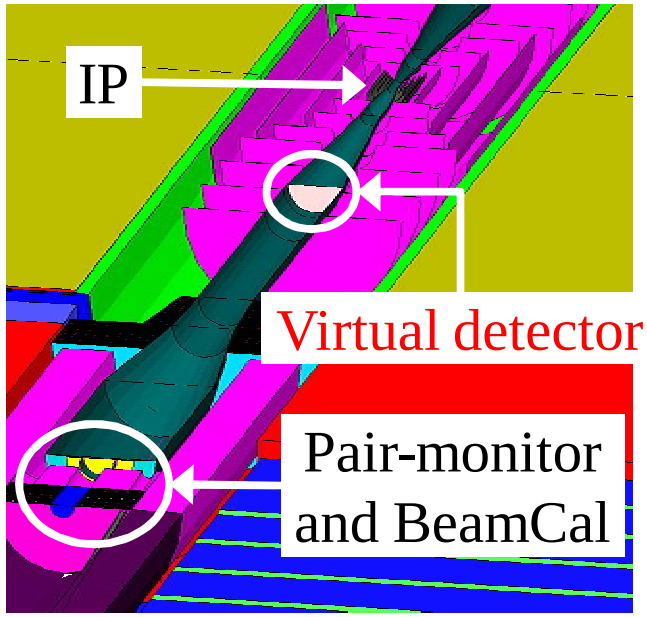
The noise level is stable (does not changed greatly).

Pair-monitor for Belle II ?

The availability of the pair-monitor for B-physics experiment @KEK (Belle II) was studied.

Simulation Setup

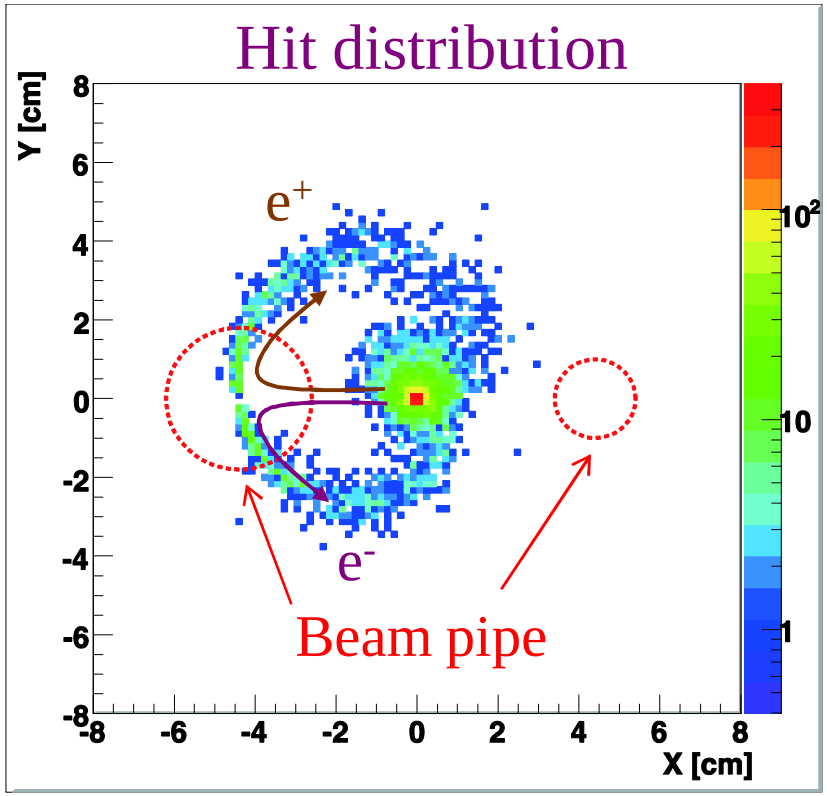
- Tools
  - CAIN (Pair-background generator)
  - Jupiter (Tracking emulator)
- Virtual detector 1.1 m away from IP.

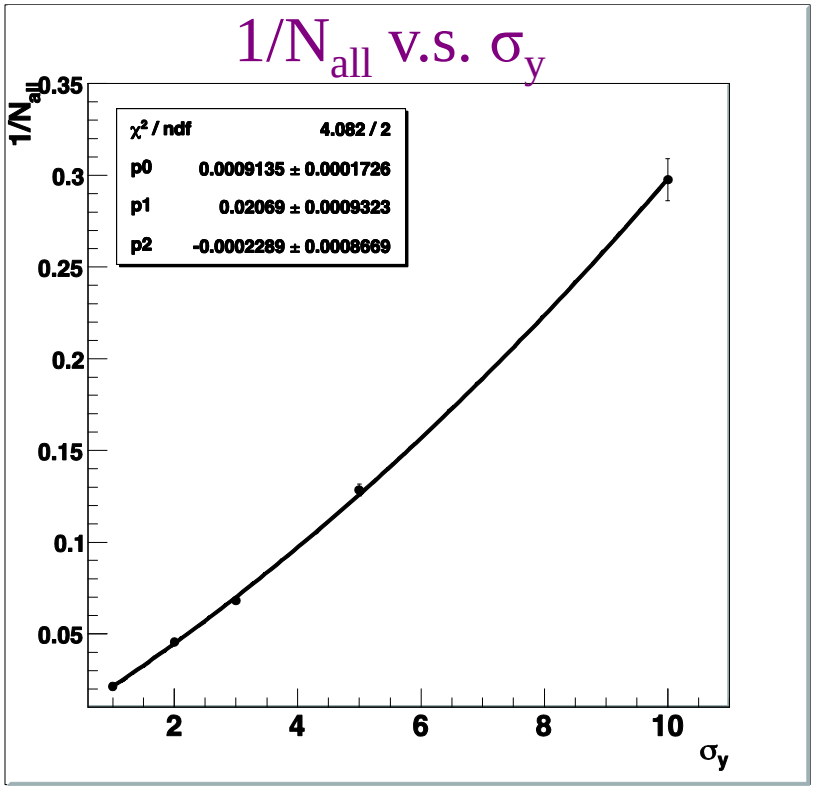


	ILC	Belle II
Beam energy	250 GeV	7.5 / 4.0 GeV
Crossing angle	14 mrad	80 mrad
Bunch size (σ_x, σ_y, σ_z)	(639nm, 5.7nm, 300μm)	(6.2 μm, 23.7 nm, 3 mm) (10.6 μm, 26.9 nm, 3 mm)
Magnetic field	3.5 T + anti-DID	1.5 T

Hit distribution of pair background

The hit distribution of the pair-background was checked (@200bunches).





→ The total number of hits (N_{all}) has information of σ_y.

Principle demonstration of the pair-monitor seems to be possible.
To be more precisely studied.

Summary

- Pair-monitor is a silicon pixel detector

  to measure the beam profile at IP.
- The development of the pair-monitor with SOI technology was started.
  - The first prototype which is only readout ASIC was produce.
  - The operation test was performed.
    - All the ASIC components work correctly.
    - The noise level is much smaller than typical signal level.
- The availability of the pair-monitor for Belle II was checked.
  - Principle demonstration of the pair-monitor seems to be possible.
  - To be more precisely studied.

Plan

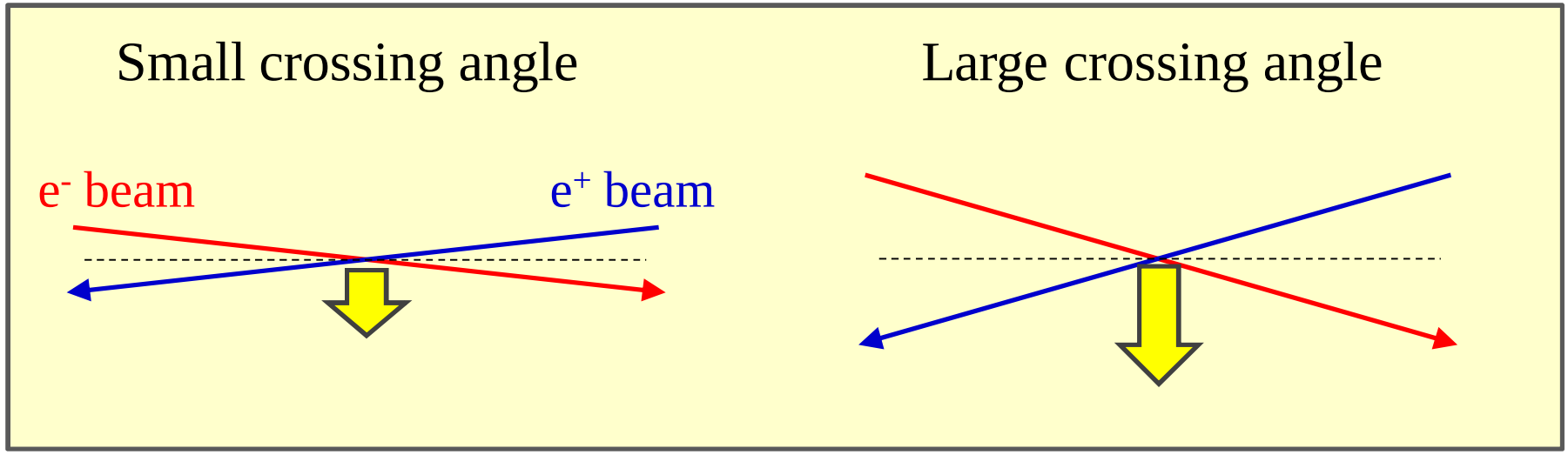
- The irradiation test will be performed next month.

Thank you for listening!

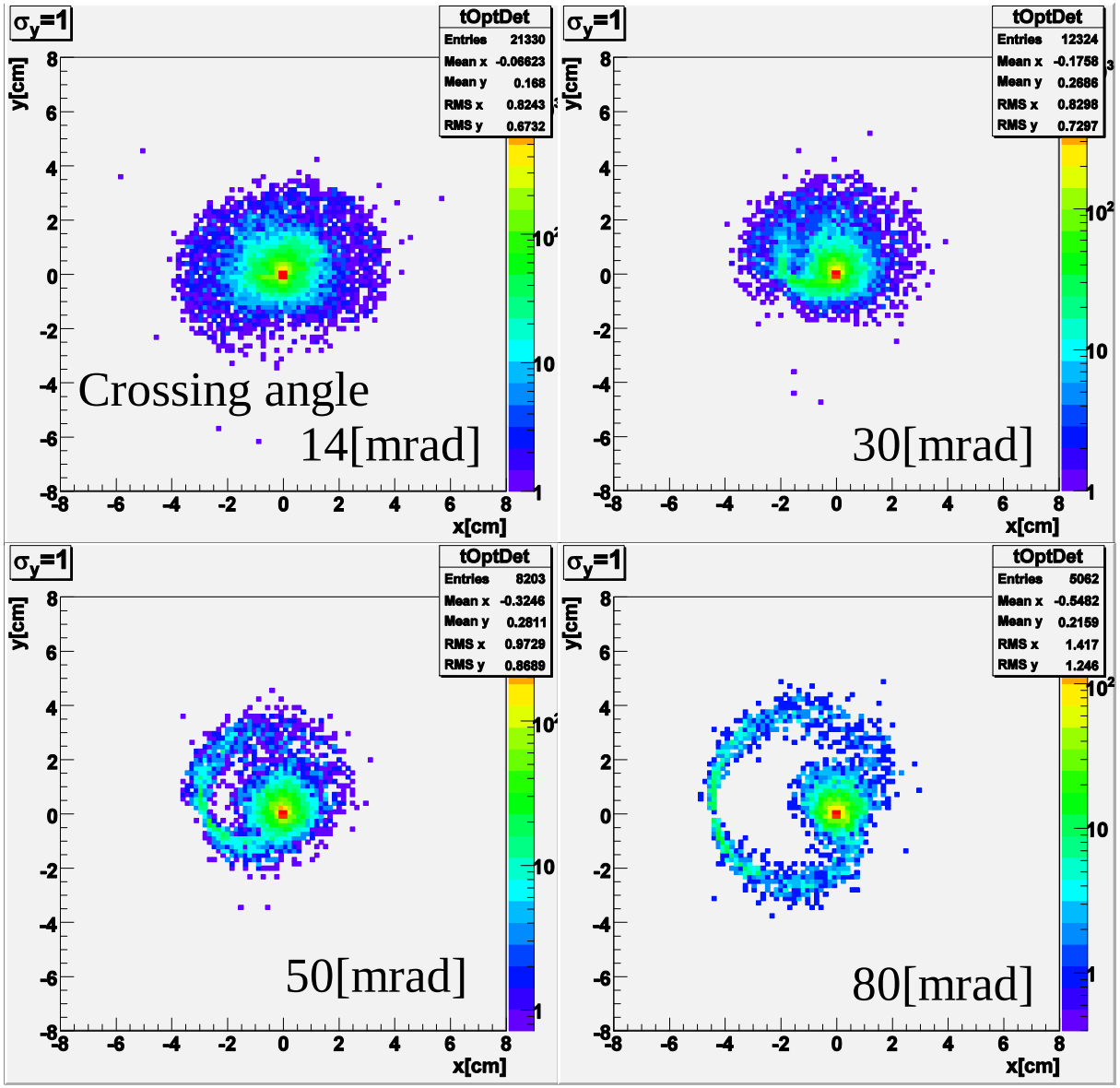
Backup

Crossing angle

- Large crossing angle leads to high momentum (p_x).



Nominal e^+e^- hit



Total number of hits