Development of Readout ASIC for FPCCD Vertex Detector

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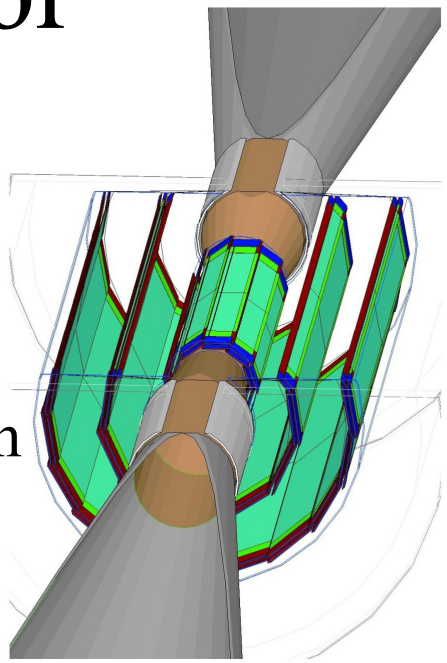
FPCCD Vertex detector



- FPCCD Vertex detector
  - FPCCD (Fine Pixel CCD)
    - Pixel size : 5 μm × 5 μm
    - Epitaxial layer thickness(Full depleted) : 15 μm
  - # of channel : 6,080 ch
    - 20,000 × 128 pix/ch
  - # of pixel : ~10^{10} pixel

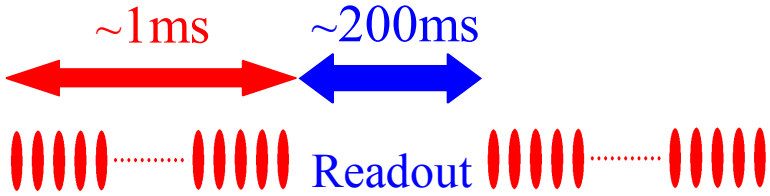
- There are quite a lot of pixels.

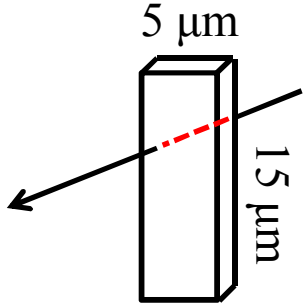
  → Multichannel readout ASIC is necessary to realize FPCCD Vertex detector.

⇨ The multichannel readout ASIC for FPCCD is developed.

Requirements for readout ASIC

- There are 3 requirements for the readout ASIC
  - Power consumption < 6 mW/ch
    - ➢ Sitting in a cryostat
    - ⇨ Total power consumption < 100W
      - 100 W/6,080 ch – 10 mW/ch
  - Readout rate > 10 Mpix/sec
    - ➢ Readout in the inter-train time
    - ⇨ 20,000 × 128 pix / 200 ms
  - Noise level < 30 electrons
    - ➢ Signal becomes small for particles penetrating with large angle





Signal becomes small

⇨ **For these requirements, measures were devised.**

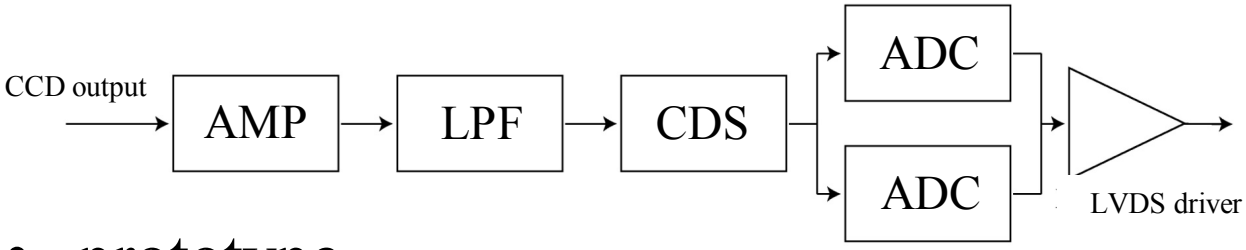
Measures for requirements

- Power consumption < 6 mW/ch
  - The main source of the power consumption : ADC, Driver circuit for signal output
  - ➢ Charge sharing ADC : < 10 μW/ch
  - ➢ LVDS output : < 2 mW/ch
  - ⇨ The power consumption of readout ASIC will satisfy requirement.
- Readout rate > 10 Mpix/sec
  - ➢ 5 Mpix/sec ADC x2
- Noise level < 30 electrons
  - ➢ Low pass filter and correlated double sampling are used.

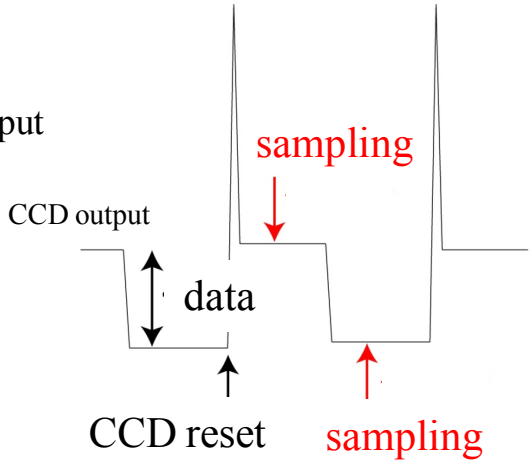
→ **The readout ASIC has been designed based on these design considerations.**

Prototype ASIC

- Design of the readout ASIC (1 channel)

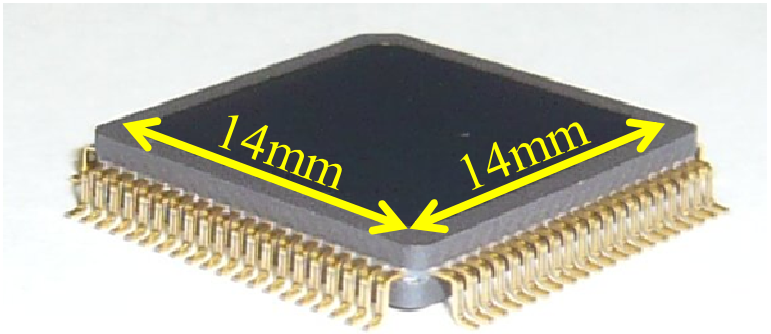


Correlated double sampling



- prototype
  - 0.35μm TSMC process
  - Chip size：2.85 mm × 2.85 mm
  - # of pad：80
  - # of channel：8
  - package：QFP-80

Readout ASIC with package

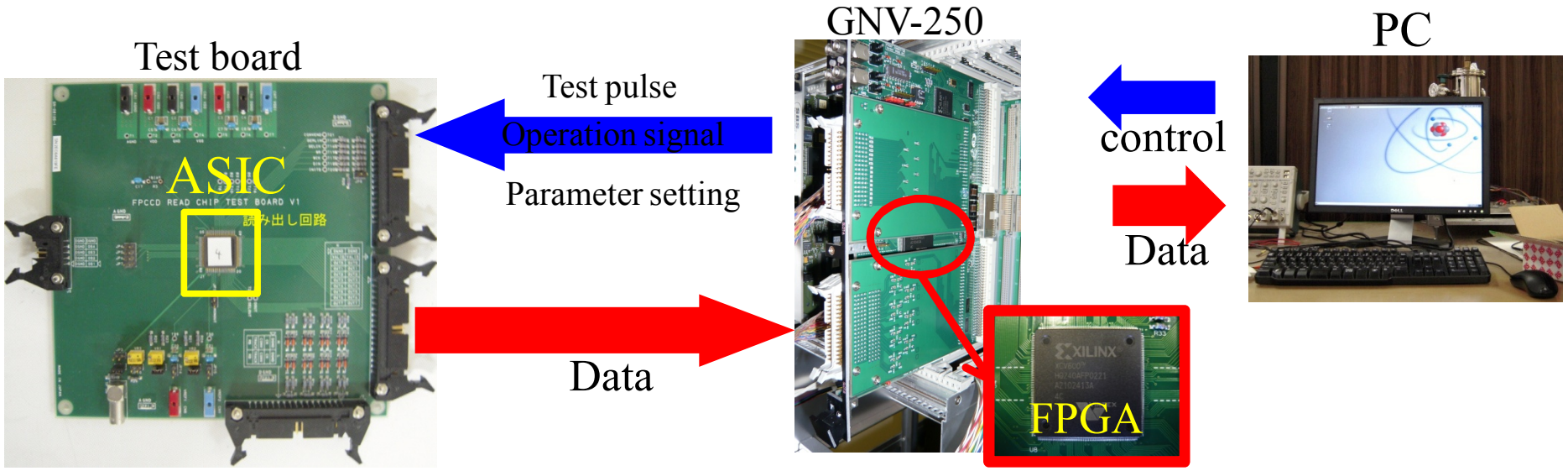


→Performance of the prototype ASIC was tested.

Performance test

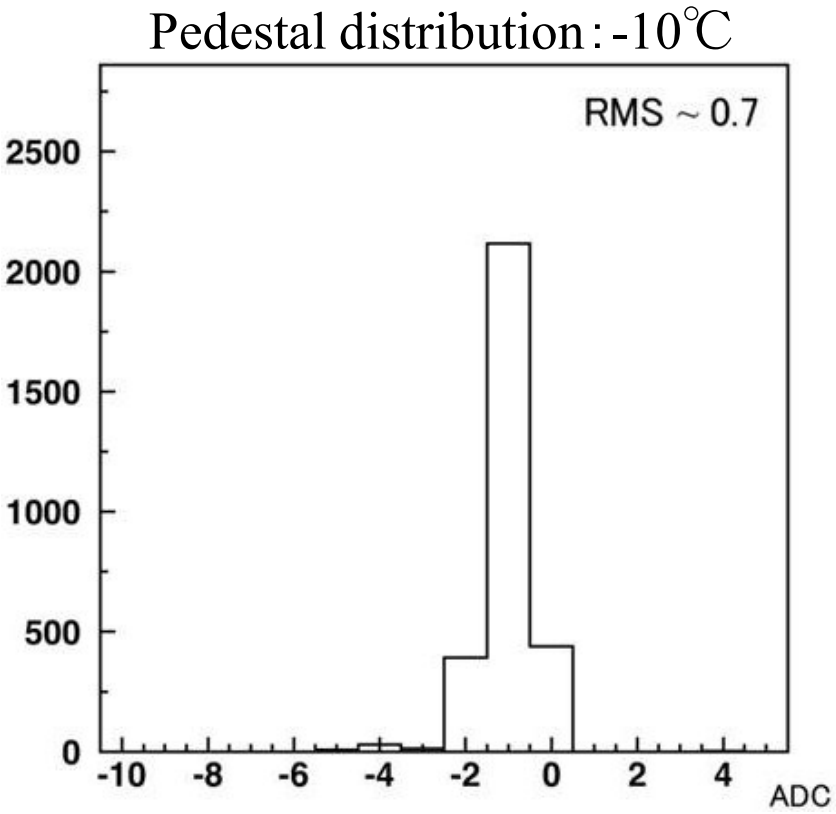
Test bench

- Data acquisition and circuit operation are done by a VME system.
  - GNV-250 module has FPGA.
    - The control logic was implemented into an FPGA.
  - The test job and parameter setting are controlled by a PC.
  - ADC information is stored in FIFO located in the FPGA, and sent to the PC.



Noise Level check

- **Pedestal distribution**
  - Readout rate ~1.5 Mpix/sec



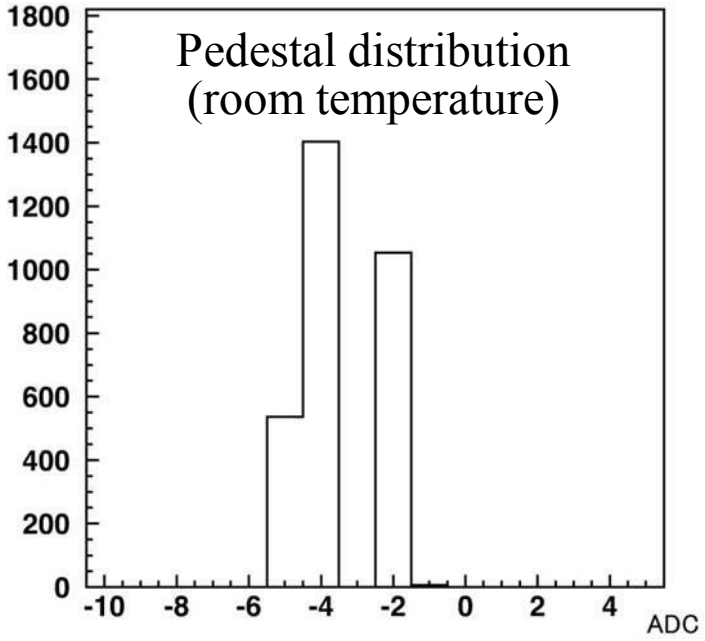
- **Noise level**
  - RMS = 0.7 ADC count ~ 28 e

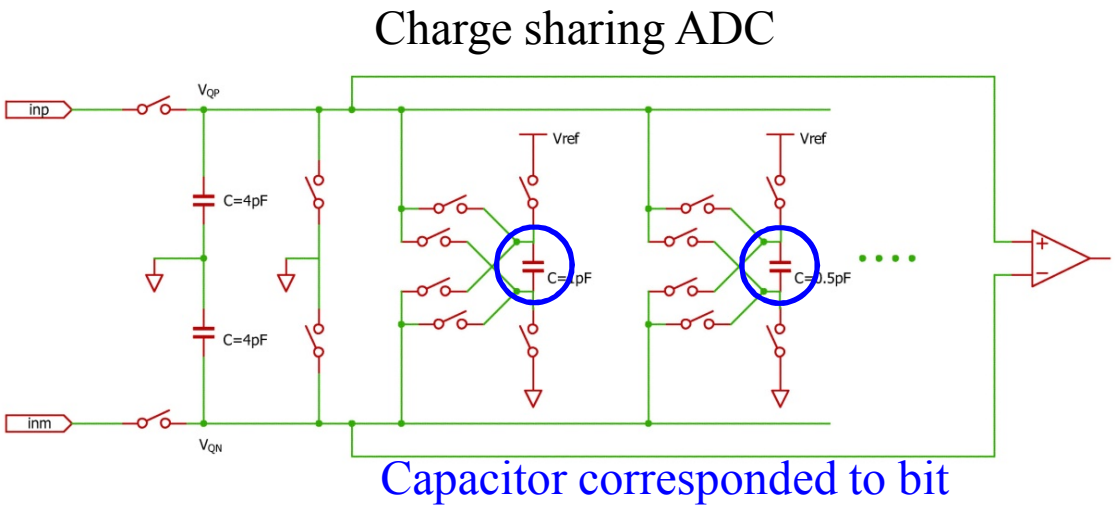
(requirement:30e)

→ **Noise level satisfied the requirement.**

Improvement of ADC

- **Some ADC counts are missing.**





➢ The capacitor in ADC seems to be shifted from design value.

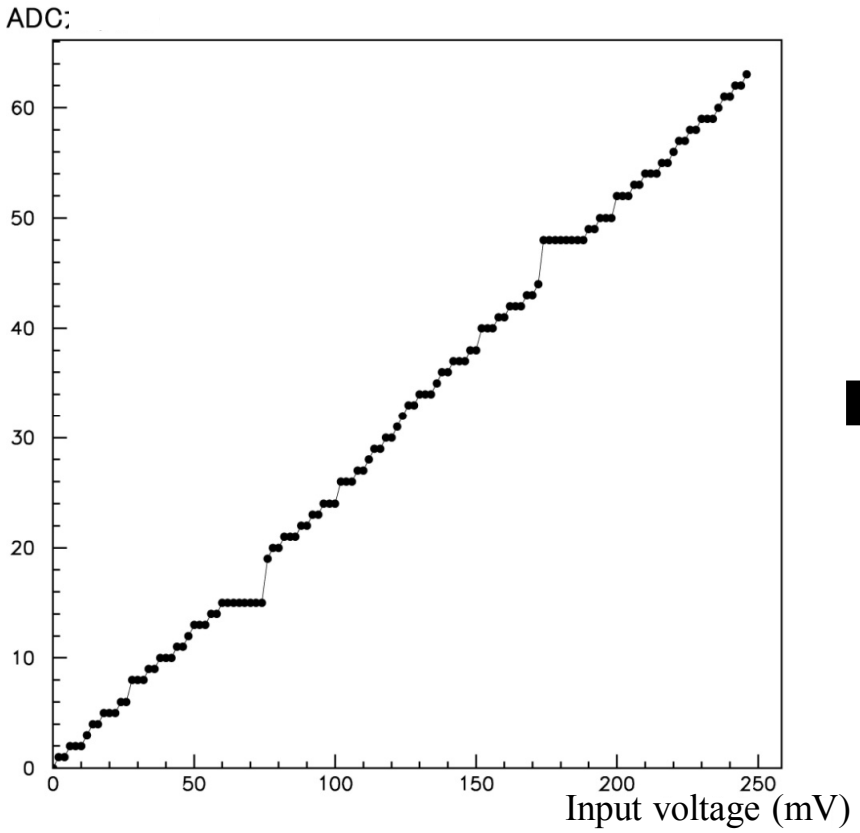
– The stray capacitance in the switching circuits

→The number of the transistors used in the switch is arranged to be proportional to the capacitance.

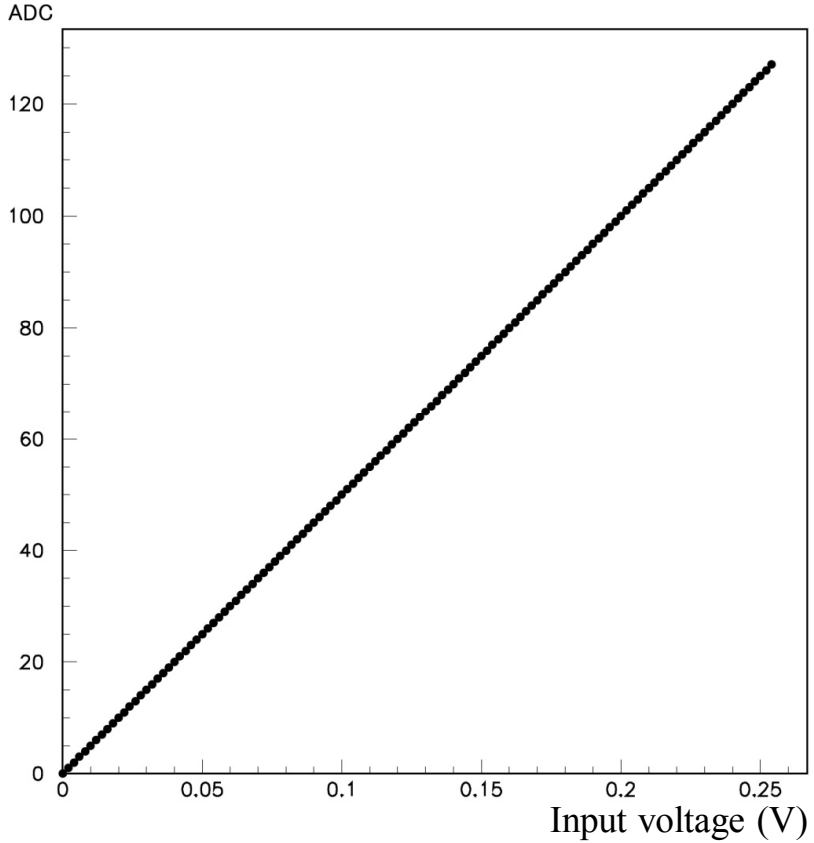
ADC simulation

- **ADC output was checked with SPICE simulation**

Present ADC



Redesigned ADC



- **At redesigned ADC, all ADC counts are output.**

→ In next ASIC, the problem will be solved.

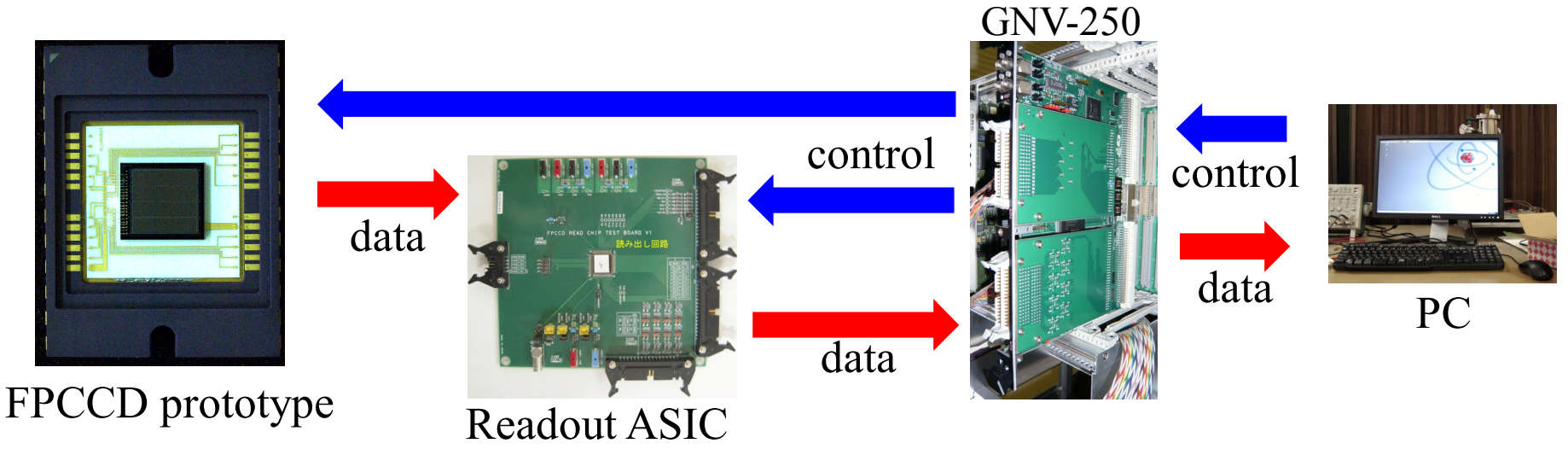
FPCCD readout

Test bench

- Readout ASIC worked almost perfectly.

⇨ A FPCCD prototype sensor was read out by the prototype ASIC.

- Test bench is about the same setup for the performance test.



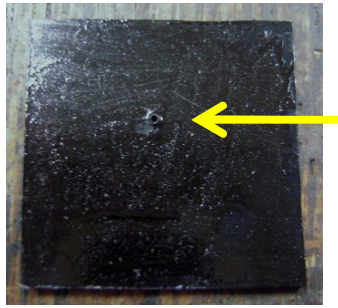
- ADC output is stored in the FIFO located in the FPGA.

➢ All the data could not be stored due to the limited memory size in the FPGA.

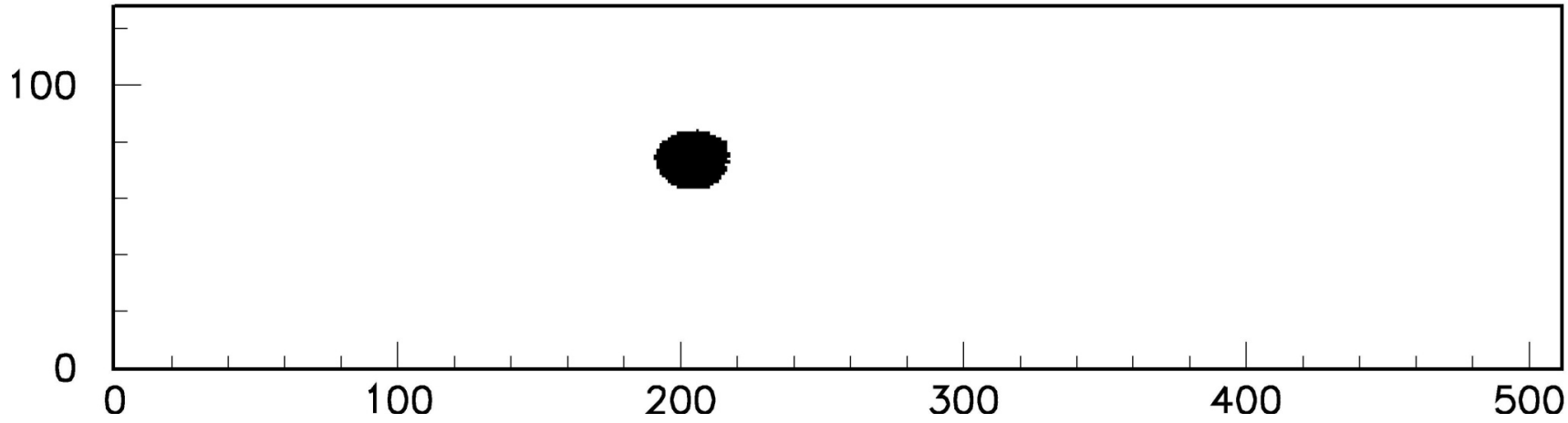
⇨ 7 bit ADC data were converted to 1bit (Threshold : 10 ADC count)

FPCCD readout

- FPCCD output was read out.
  - FPCCD was covered by a light shielding plate.
  - LED irradiation time : ~1 μs



Light shielding plate

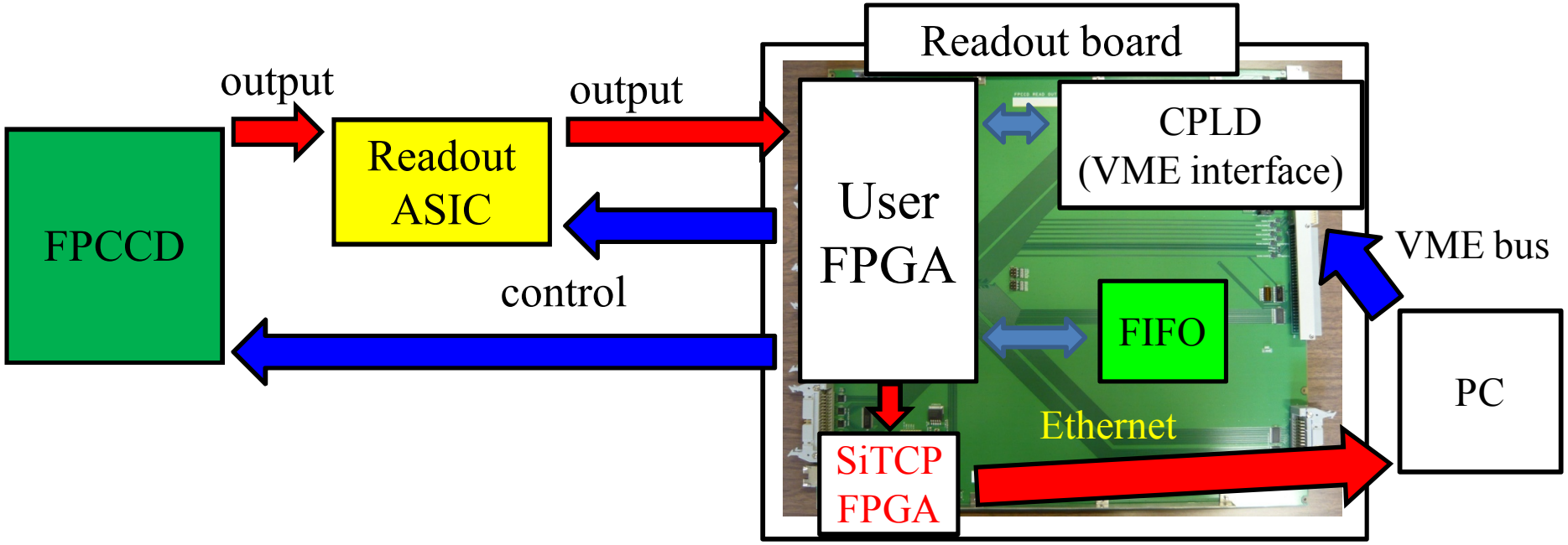


- **FPCCD image could be read out by the readout ASIC.**

Readout board

- Readout board was developed to readout all the data.
  - ➢ The data can be transferred by using Ethernet.

⇨ All the data of a FPCCD sensor can be read out.



- Performance of the readout board was checked.
- Measured transfer rate : 25 Mbps

Summary

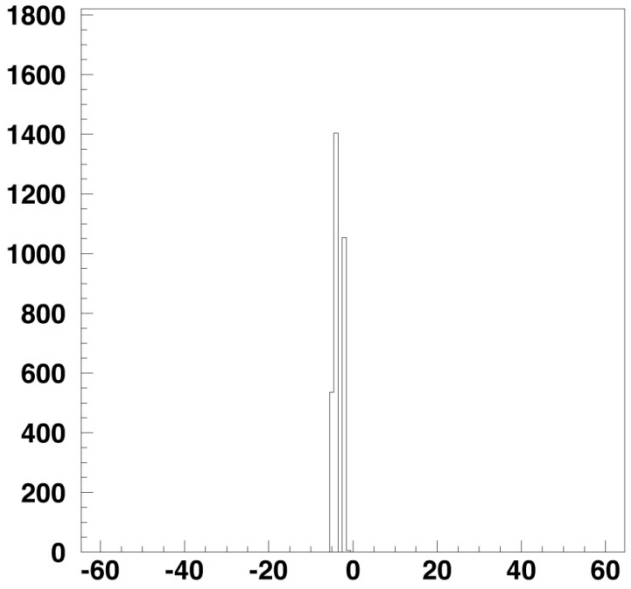
- Readout ASIC for FPCCD is developed.
- Required performance
  - Power consumption < 6 mW/ch
  - Readout rate > 10 Mpix/sec
  - Noise level < 30 electrons
- The performance of the readout ASIC was checked.
  - Noise level ~ 28 electrons
  - Some ADC counts are missing.

⇨ Next prototype will be made this year.

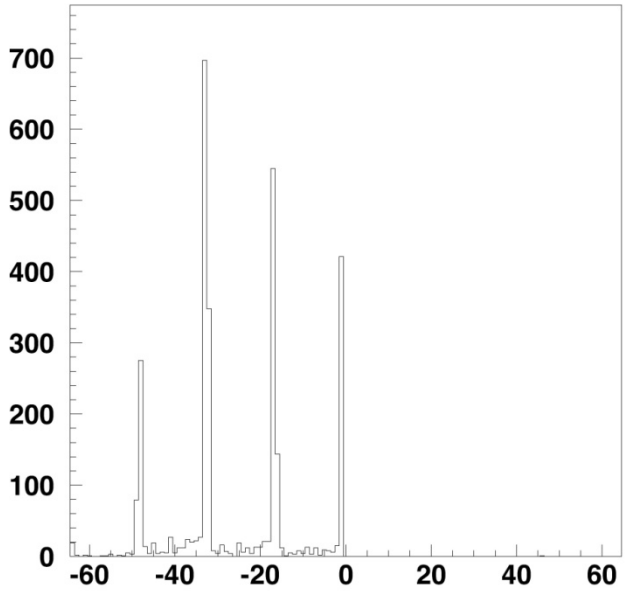
- The prototype readout ASIC can read out a FPCCD sensor.
  - To read out all the data of a FPCCD, the readout board was developed.

Readout rate

Pedestal distribution
Readout rate ~ 1.5 Mpix/sec

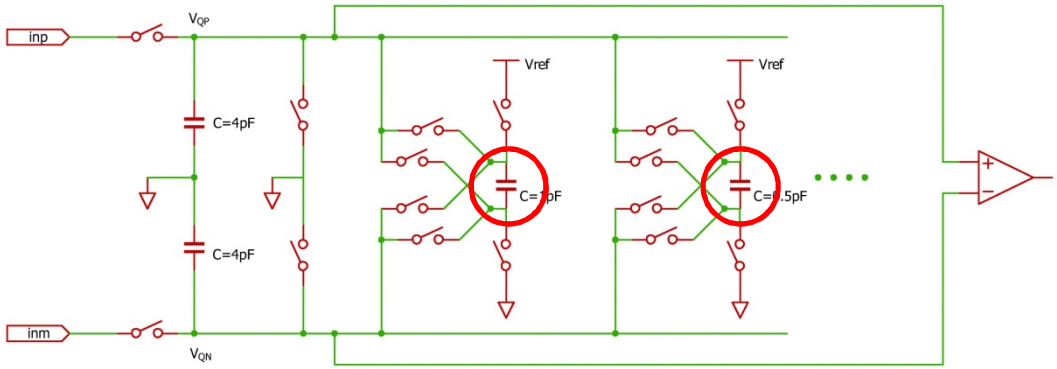


Pedestal distribution
Readout rate ~ 5 Mpix/sec

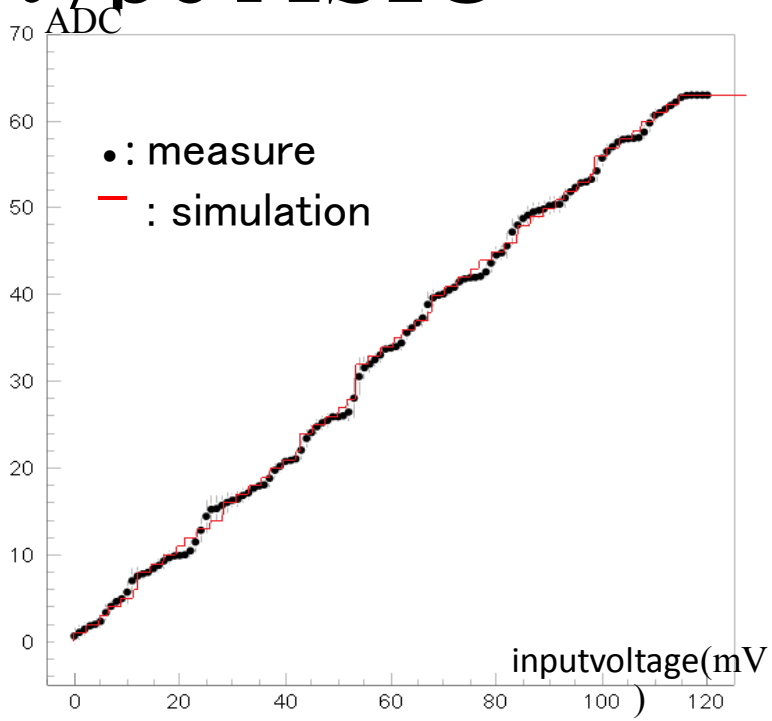


Problem of prototype ASIC

- Some ADC counts are not output.
- Possible cause : ADC capacitor was changed from design value.



- A/D conversion of enlarged capacity of ADC capacitor was simulated by Scilab.



- Simulation result is consistent with measurement.
- Because of floating capacitance, ADC capacitor was enlarged.
- For the next prototype, ADC was redesigned.