Development of software for FPCCD vertex detector

Tohoku University

Daisuke Kamai

FPCCD vertex detector

FPCCD vertex detector

Prototype of FPCCD

■ FPCCD(Fine Pixel CCD)

   – Pixel size : 5μm x 5μm

   – Thickness : 15μm

■ The number of pixels : ~10^{10} pixels

→The small pixel size enables to reject background hits by using the cluster shapes.
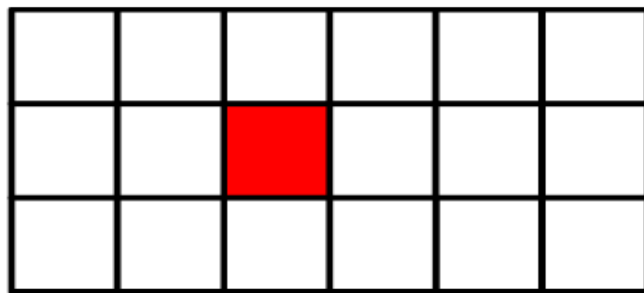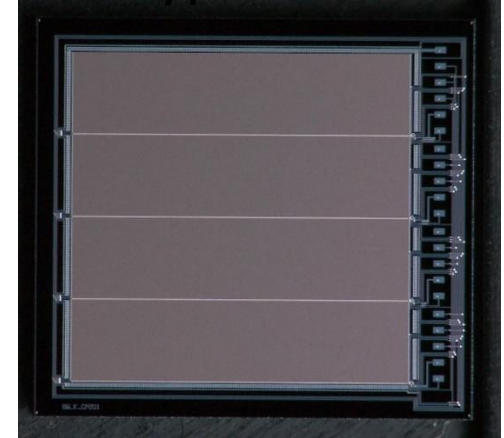
Large pixel size
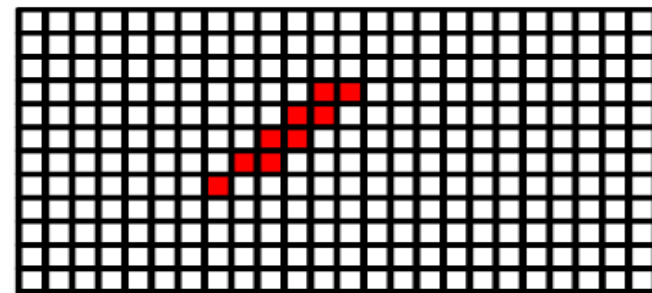
FPCCD

Software for FPCCD

Purpose of this study

- Estimation of the pixel occupancy by pair-background.

- Development of an algorithm to reject background hits based on the cluster shapes.

- Evaluation of the tracking and vertexing performance.

→ For this purpose, software for FPCCD vertex detector is developed.

- FPCCD digitizer
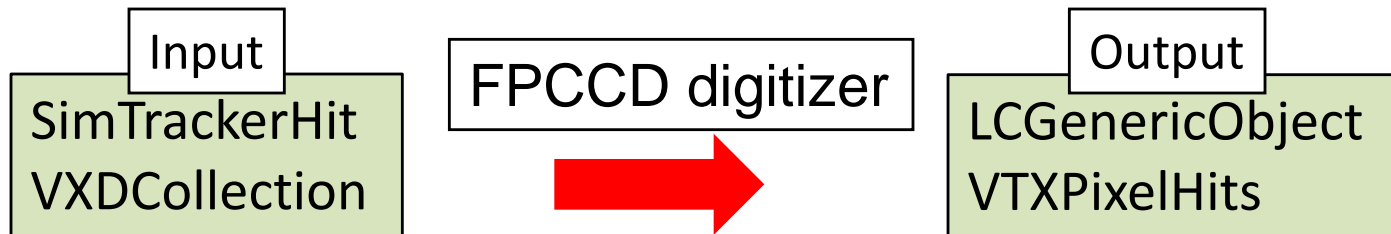- Overlay processor

Today's talk

- FPCCD clustering
- FPCCD track finder
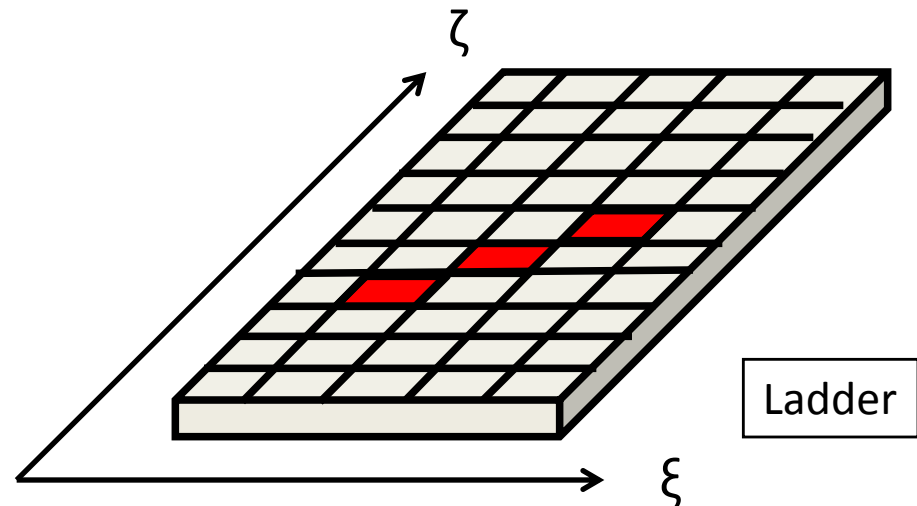
FPCCD digitizer

FPCCD digitizer

— FPCCD has a large number of pixels.

— The digitizer specialized for FPCCD is necessary.

Input		Output
SimTrackerHit VXDCollection	FPCCD digitizer ➡	LCGenericObject VTXPixelHits

— The hit information of a FPCCD ladder is packed in one element.

Members of VTXPixelHits

☐ Layer number (0~5)
☐ Ladder number (0~16)
☐ ID of ξ (0~4400)
☐ ID of ζ (0~50000)
☐ Energy deposit (float)
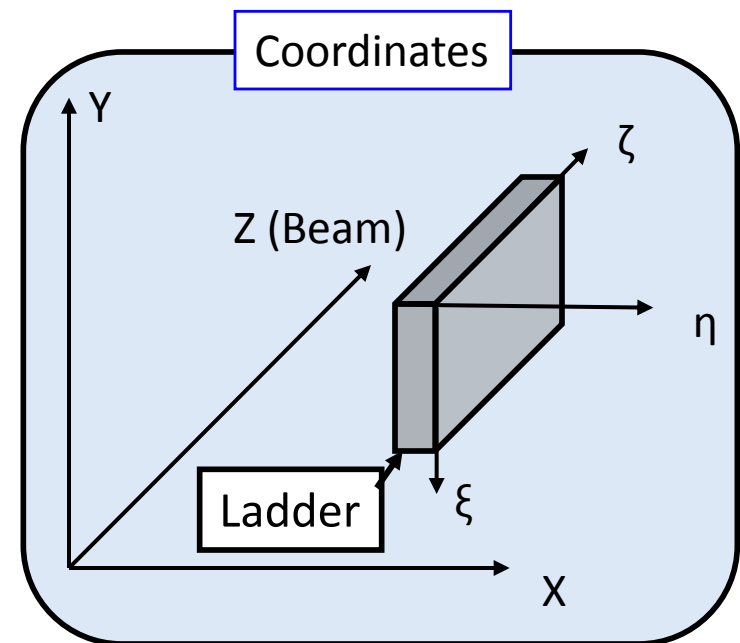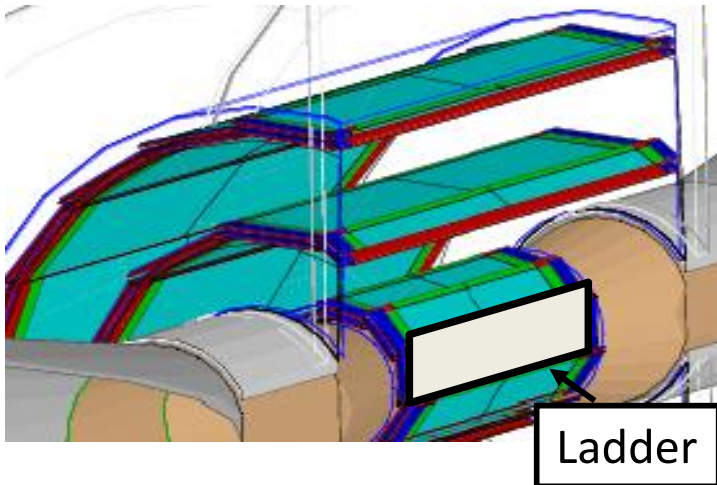☐ Hit quality (0~3)

ζ

ξ

Ladder

Algorithm of FPCCD digitizer (1)

- The hit points and track momenta are obtained from SimTrackerHit.
  - posX = SimTrackerHit->getPosition()[0];
  - momX = SimTrackerHit->getMomentum()[0];

- The hit points and momenta are transformed to the local coordinates on a ladder.

Ladder

Coordinates

Y

ζ

Z (Beam)

η

Ladder

ξ

X

Algorithm of FPCCD digitizer (2)

■ The track is calculated by the local point and local momentum.
  — Large momentum → Approximated by a linear track.
  — Low momentum → Calculated as a helical track.
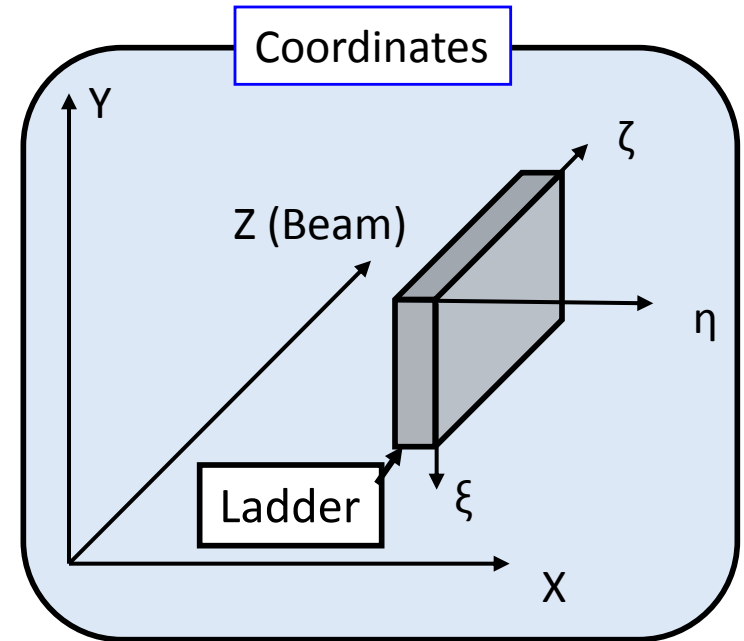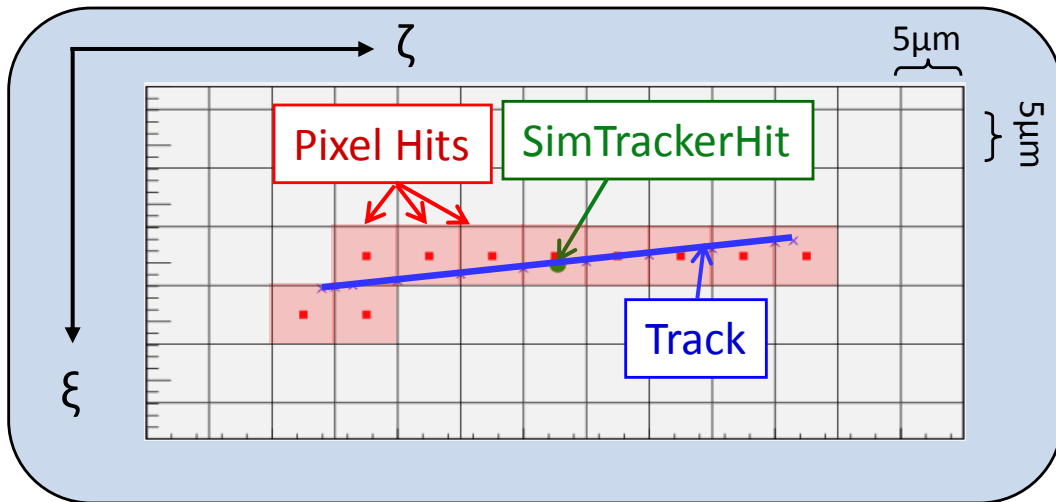
■ The energy deposit in SimTrackerHit is calculated by using the path length in each pixel.

Output collection from FPCCD digitizer

Format of LCGenericObject

■ The first word(32 bits) contains layer number and ladder number of the element.

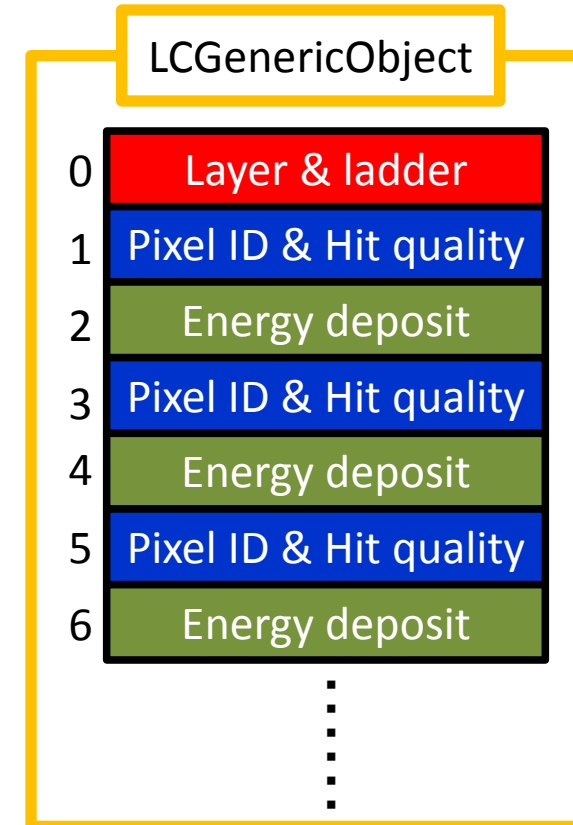| Blank	Blank	Layer(8bits)	Ladder(8bits)

■ Two words are used for each pixel hit.

		ID of ξ(13bits)	ID of ζ(16bits)

Hit quality(2bits)

Blank(1bit)

Energy deposit (32bits)

LCGenericObject

0	Layer & ladder
1	Pixel ID & Hit quality
2	Energy deposit
3	Pixel ID & Hit quality
4	Energy deposit
5	Pixel ID & Hit quality
6	Energy deposit
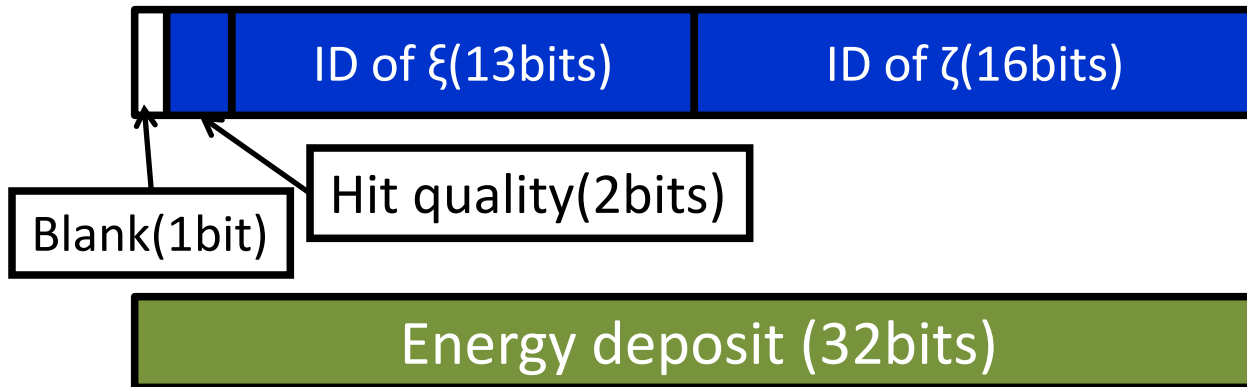
— The number of elements is equal to that of the ladders with hits.

— Data size for one element : $(2 \times N_{hits} + 1)$ words

— The blank area is reserved for the future use.

Development of Overlay processors

- **OverlayEvents**

  The number of the pair-backgrounds for 1 BX is too large to include in one event.

  – Divided into about 1800 events in Mokka run.

  →OverlayEvents processor was newly developed to merge these events to a single event record.

- **OverlayBX**

  – OverlayBX processor was modified to merge VTXPixelHits.

  – If there are more than 2 hits in the same pixel, the processor adds the energy deposit and rewrites Hit quality.

  – Hit quality : Single signal hit,

    Multiple signal hits,

    Multiple hits by the signal and background,
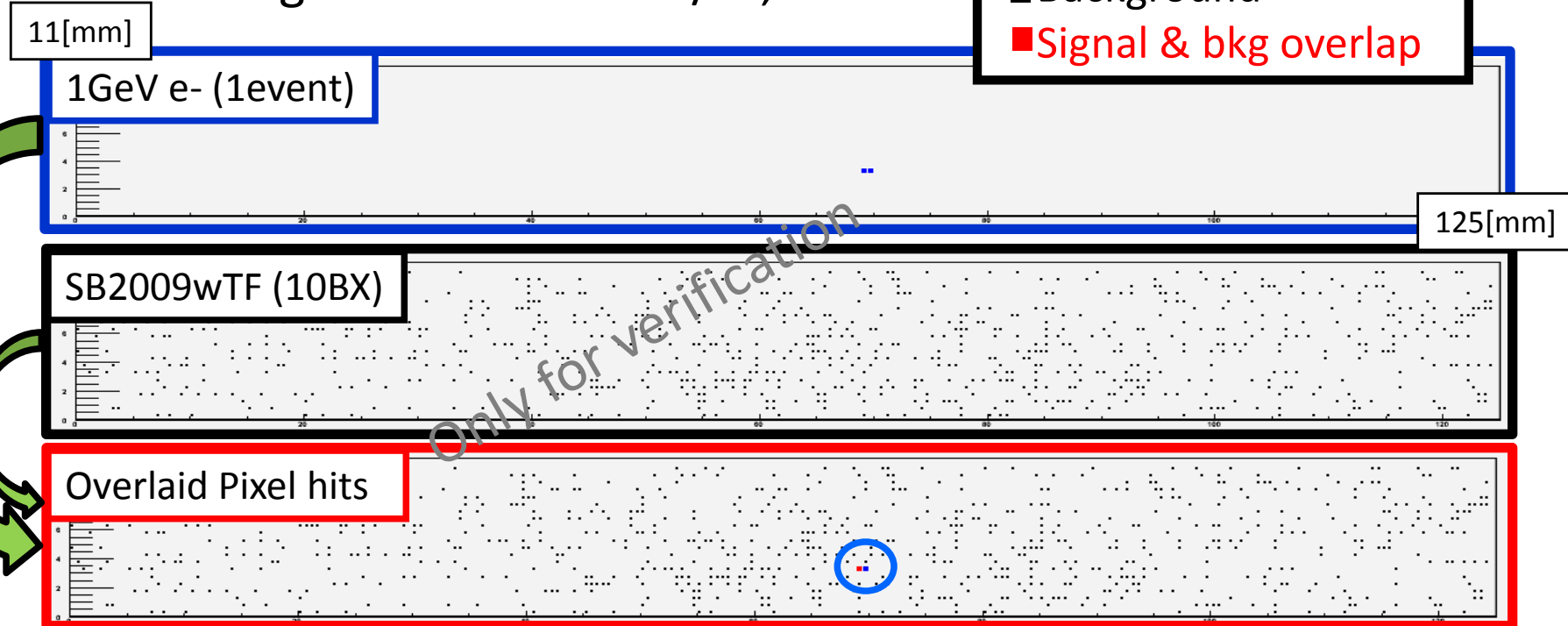
    Background hits.

Test of OverlayBX processor

<u>OverlayBX for VTXPixelHits was tested.</u>

■ The pixel hits on one ladder of the innermost layer are plotted.
  — Pixel size : 500 μm × 500 μm (to make easily to see)
  — Signal : e-, 1 GeV, 1 event
  — Pair-background : SB2009w/TF, 10BX

■ Single signal
■ Background
■ Signal & bkg overlap

11[mm]

1GeV e- (1event)

125[mm]

SB2009wTF (10BX)

Overlaid Pixel hits

Only for verification

The pixel hits are merged correctly.

Estimation of pixel occupancy

The pixel occupancy of the FPCCD VTX <u>innermost layer</u> was checked.

— Pixel size : 5µm × 5µm

— Thickness : 15µm

Background conditions
— Generator : Guinea Pig
— Beam parameter :
SB2009w/TF
— CM energy : 500 GeV
— Range cut : 0.1 mm

Pixel occupancy of the innermost layer vs #BX
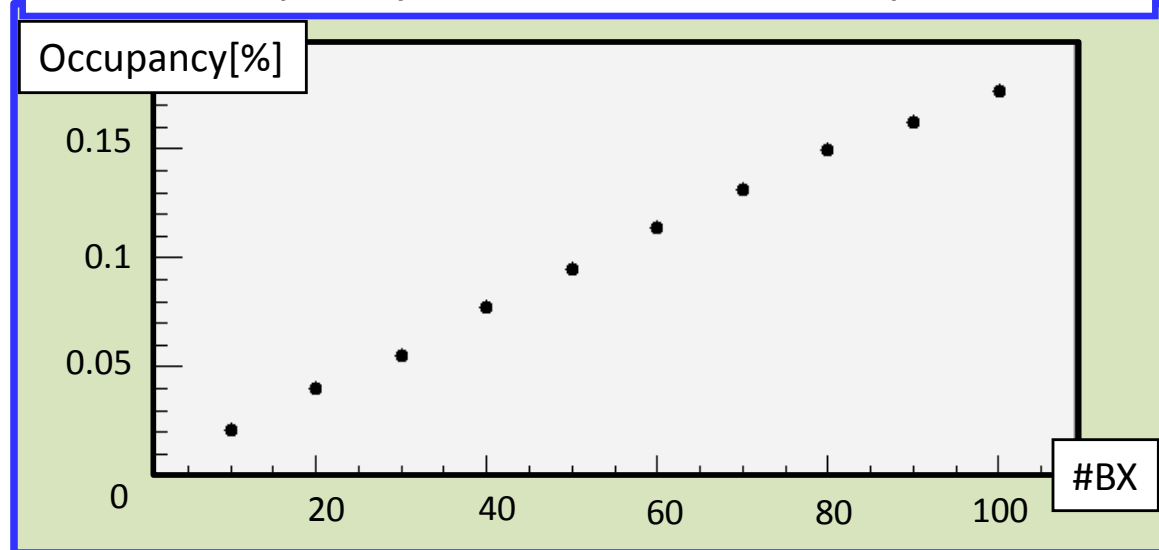
Expected pixel occupancy : ~2.5% for 1train(1312 BX)

The occupancy is about a half of the previous result.

(In the previous study, the overlap hits were not considered.)

Data size & memory usage

Data size of pair-background events

■ Merged data (1 event) : 25 MB/BX.

(Separated data(1800 events) : 40 MB/BX.)

→Data size of VTXPixelHits : 130MB for 1 train.

We will be able to study performance in a realistic condition.

Performance of processor

■ Amount of memory used for running processor.

— FPCCD Digitizer : 190 MB

— OverlayEvents : 400 MB

— OverlayBX :   ~2GB for 1 train

(~300MB for 50BX, ~400MB for 100BX)

→ It is acceptable.

Summary / Plan

Summary

■ We developed software for the FPCCD vertex detector.
— The FPCCD digitizer and Overlay processor were developed.
— The performance of the FPCCD vertex detector can be studied with background by using these software.

Plan

■ FPCCD clustering
— Development of FPCCD clustering is getting started.
— Algorithm to reject background hits based on the cluster shapes will be developed.
■ FPCCD track finder
— FPCCD track finder will be developed.