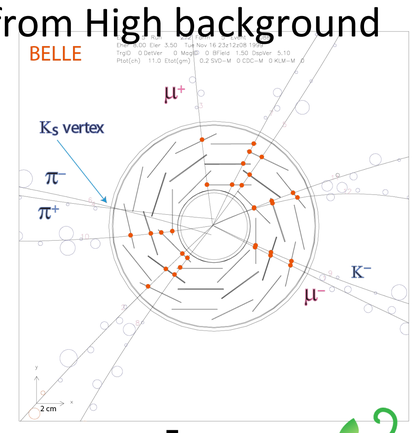
Development of the Pixel OR SOI Detector for High Energy Physics Experiment

Y. Ono, A. Ishikawa(Tohoku Univ), Y. Arai, T. Tsuboyama(KEK), Y. Onuki(Tokyo Univ),
T. Imamura, T. Ohmoto, A. Iwata(A-R-Tec Corp)

Motivation ⇒ SOIPIX

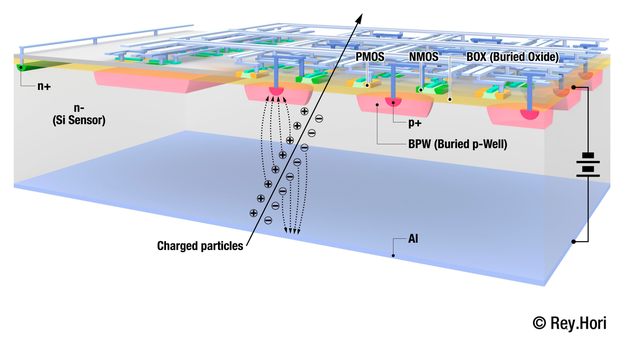
Target : Vertex detector @ High Energy Experiment
- Search vertex point of the b/c-quark particle decay
  - ➢ Reconstruct charged particle track
  - ➢ Separate effective event from High background

WANTED
- High point resolution
- Low Occupancy
- Low Material Budget
- ...etc



SOI PIXel detector (SOIPIX)

SOI(Silicon On Insulator) wafer substrate = "Sensor"



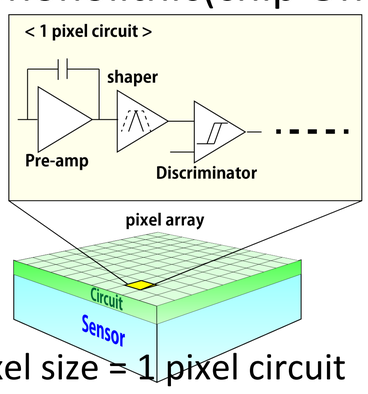
Monolithic detector
- ➢ low material budget
- ➢ High S/N
- ➢ complex functions in a Pixel
- ➢ High yield (∵No Bump Bonding)

SOI CMOS readout
- ➢ low power operation
- ➢ stability for wide temperature
- ➢ No latch up / SEQ

Suitable for vertex detector.

PIXOR Concept

But, a Monolithic(chip On Sensor) Pixel Detector is …

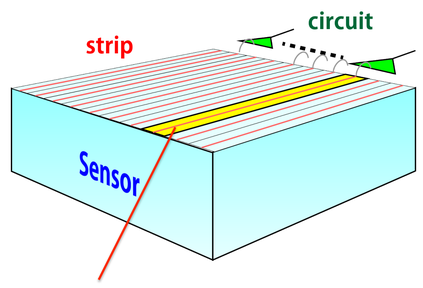


pixel size = 1 pixel circuit

Pixel => high segmentation, S/N
☺Low Occupancy
☺Low Material Budget

Mounting many functionalities on the chip, pixel size is limited by its large circuit area
☹Low point resolution

While, a Strip Detector is …

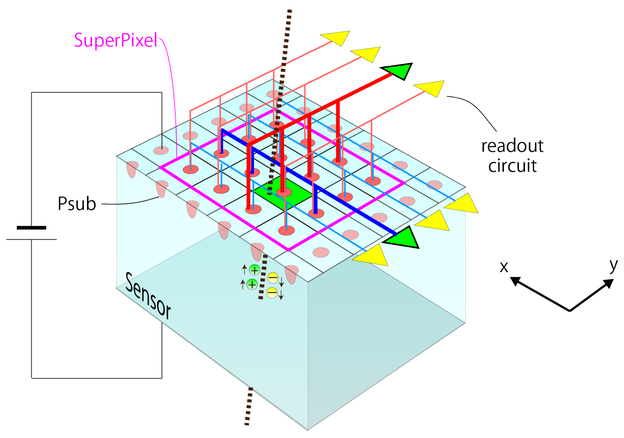


1 channel = large sensitive region

Strip => low segmentation, S/N
(comparing to a Pixel detector)
☹High Occupancy
☹High Material Budget
Large strip area⇒ no constraint for strip pitch (generally off-sensor)
☺High point resolution

~ New Readout Scheme ~

PIXel OR (PIXOR)



1. Divide signal into 2 direction (X,Y)
2. Take OR along 2 direction pixels (X,Y)
3. OR signal is processed by Readout circuit
4. **Get 2-dimensional hit information**

☝ 4 pixel OR (16 pixel => 8 channel)

Effective Circuit Number on a SuperPixel (n*n pixel): n^2 (pixel) ➡ $2n$ (PIXOR)

By sharing the circuit area with logical OR pixels, we adjust
☺ High point resolution & ☺ Low Occupancy

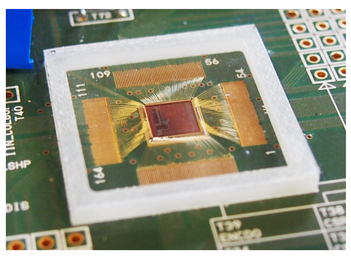
PIXOR1 Evaluation

We fabricated first prototype named "PIXOR1", and checked following 3 contents.

PIXOR1 parameter

- Binary Hit Info.(Large area)

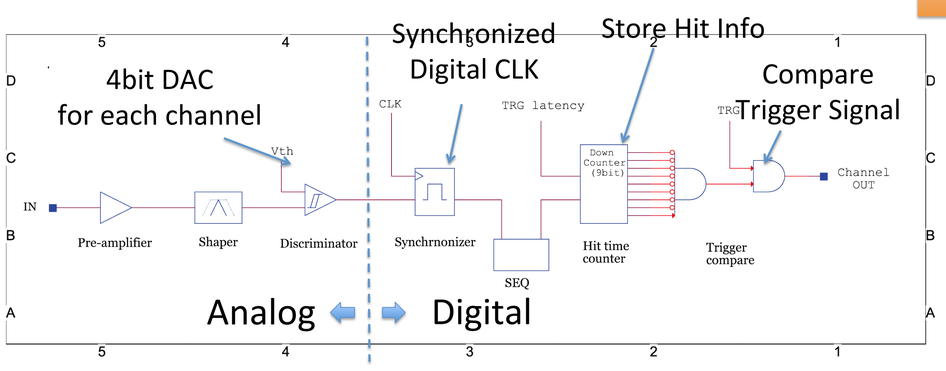
pixel pitch	25μm*40μm
pixel OR	16
Number of pix	5,632pix



Lapis 0.20um SOI process

- Shaper Output (small pixel OR block)

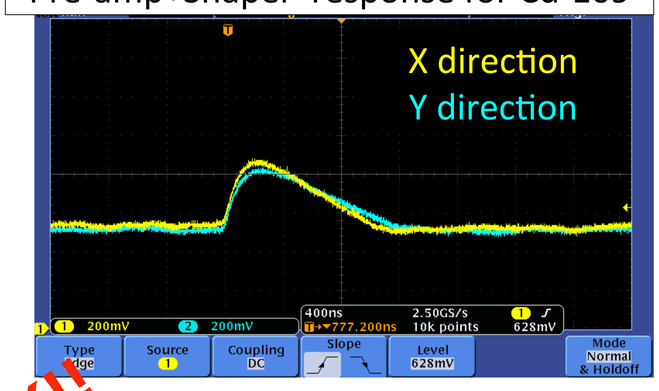
PIXOR1 circuit



Analog : Pre-amp + Shaper + Discriminator
=> Binary Readout (Hit or not)
Digital : Store hit information for trigger latency time
=> Down Counter (Hit=>Count Down)

Shaper Output

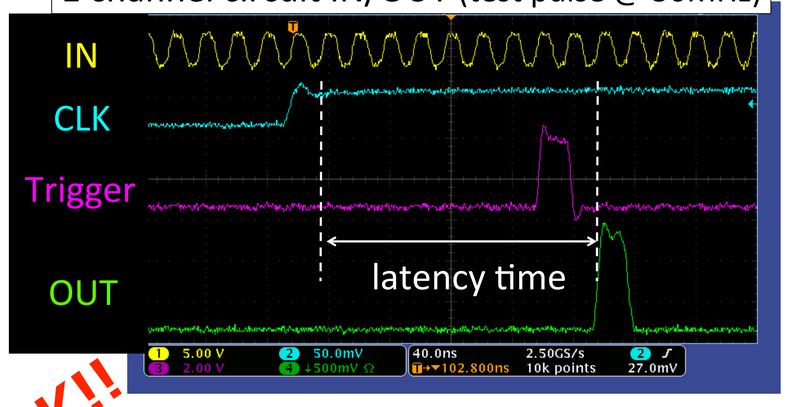
Pre-amp+Shaper response for Cd-109



OK!! Signal is equally divided into 2 directions with 2 separation diode.

Trigger Circuit

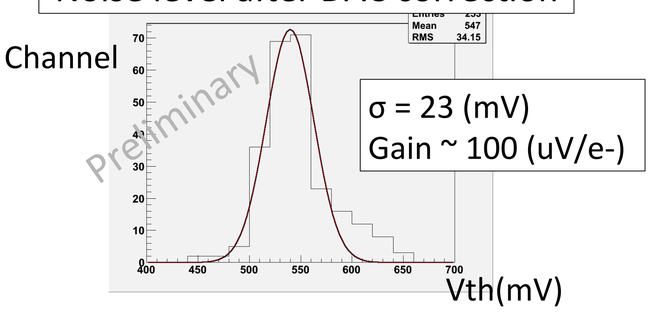
1 channel circuit IN/OUT (test pulse @ 50MHz)



OK!! Hit Information is stored at each channel for the trigger latency time.

Discriminator

Noise level after DAC correction



Noise level : ~ 230 (e-)

Future prospect

- Through a beam test, measure its efficiency , cluster size for MIP
- optimize the time constant of the Pre-amp + Shaper
- More complicated digital circuit for the trigger readout