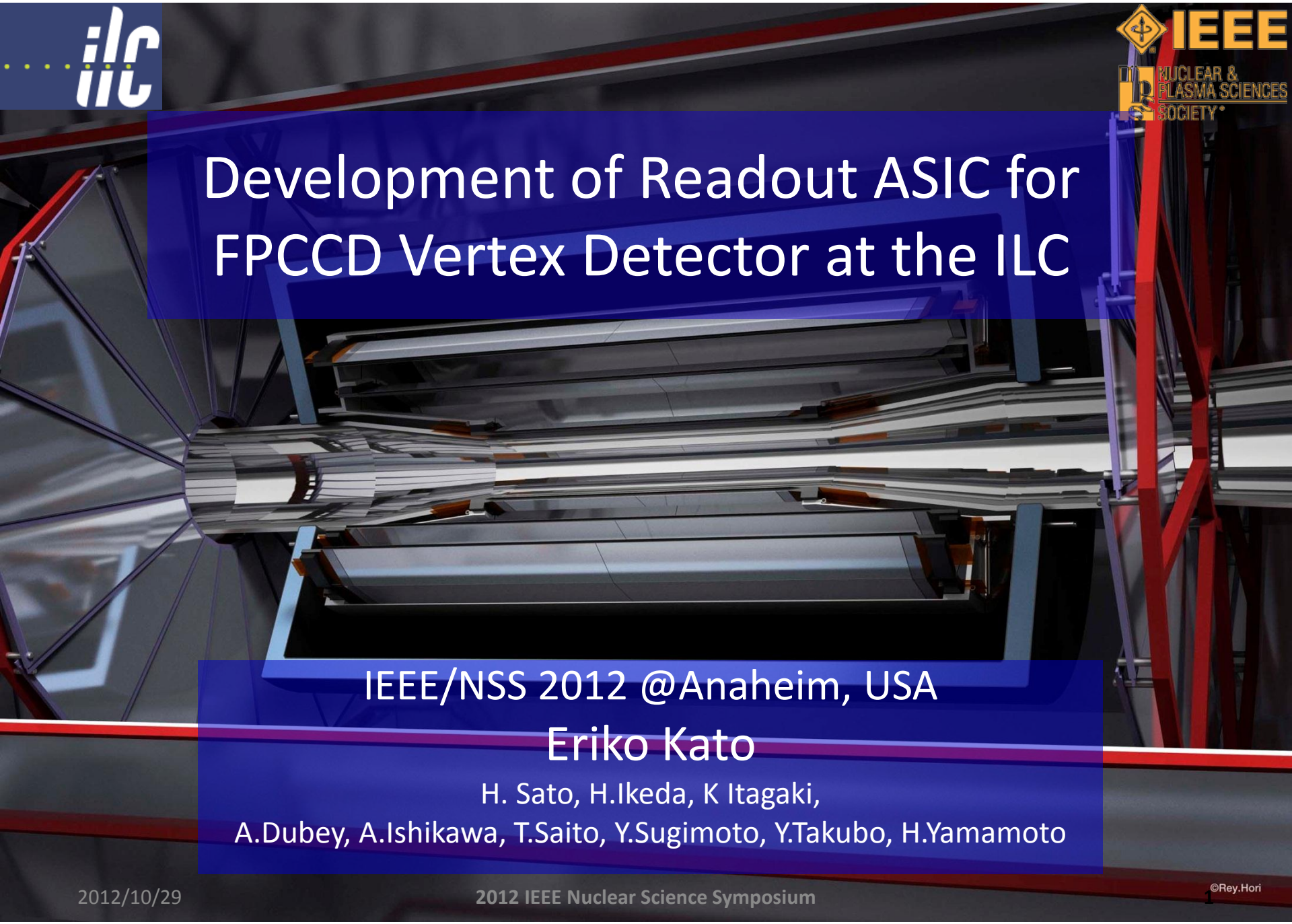


Development of Readout ASIC for FPCCD Vertex Detector at the ILC

IEEE/NSS 2012 @Anaheim, USA

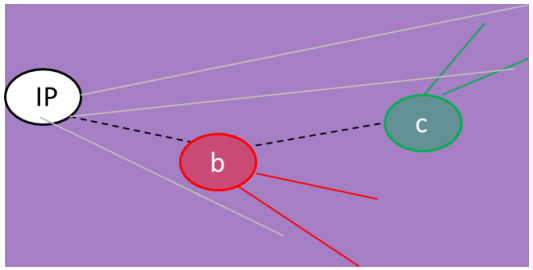
Eriko Kato

H. Sato, H.Ikeda, K Itagaki,

A.Dubey, A.Ishikawa, T.Saito, Y.Sugimoto, Y.Takubo, H.Yamamoto

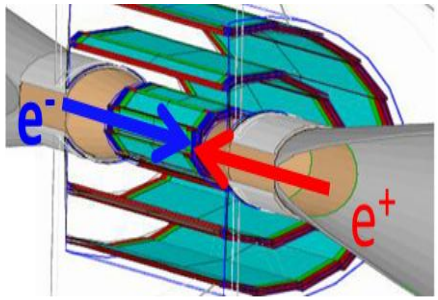
FPCCD ILC vertex detector

- ILC(International Linear Collider)
  - precision measurement of Higgs couplings
  - High efficiency, purity flavor tagging



➢ Need high impact parameter resolution

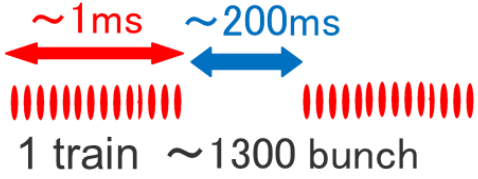
- vertex detector
  - High impact para. resolution ⇒ near IP
  - Accurate tracking ⇒ pixel occupancy~1%



➢ Finely segmented pixel

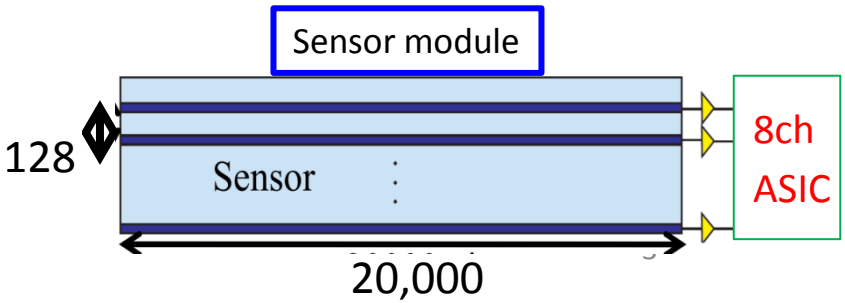
- FPCCD(FinePixelCCD) vertex detector
  - Pixel size 5x5um^2 : ☺ high position resolution, ☹ faint signal
  - total # pix: 1.6×10^{10} : ☹ high speed readout
  - Fully depleted epi-layer :15μm, Si total 50μm: ☺ high 2 track separation capability
  - inter-train time readout: ☺ free from beam induced RF noise

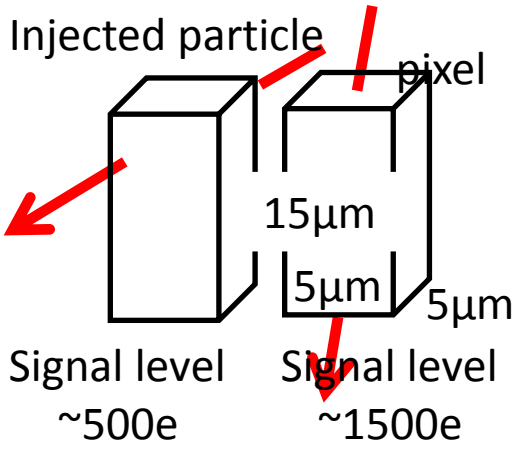
➢ Develop Readout ASIC for FPCCD



Requirements for FPCCD readout ASIC

- readout speed> 10Mpix/sec
  - 6000 ch parallel readout of
  - all pixels within inter-train time(200ms)
- signal meas. accuracy < 30 e-
  - Faint signal level : ~500 e-
  - Noise + AD conversion accuracy< 30 e-
- power consumption < 6mW/ch (ASIC)
  < 10mW/ch (CCD)
  - Placed in -40℃ cryostat

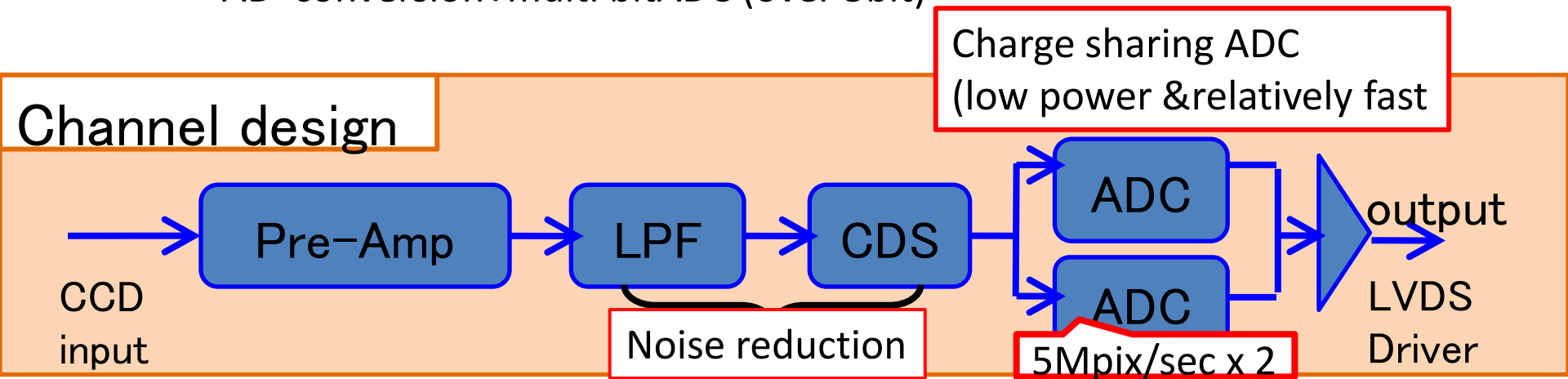




➢ Develop readout ASIC that satisfies all requirements

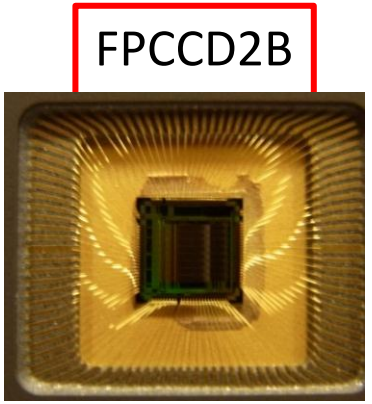
Overall ASIC design

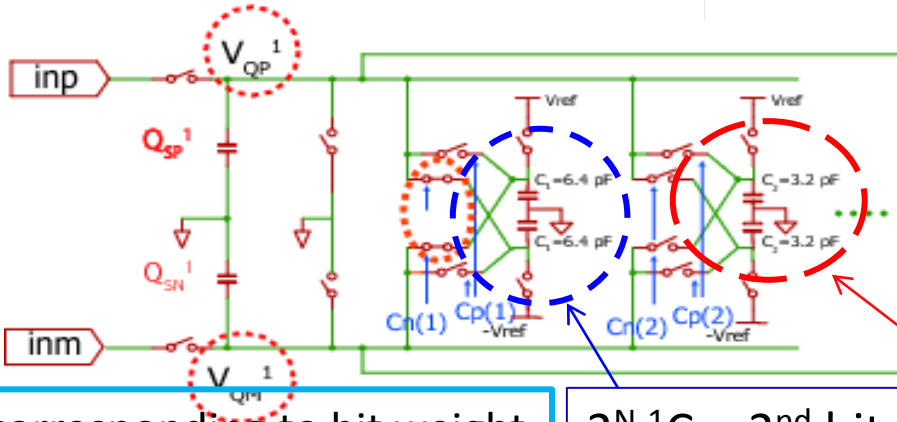
- Power consumption <6mW/ch
  - Main power source is ADC
  - Implement charge sharing ADC
- Readout speed>10 M pixel/s
  - Use two 5Mpixel/s parallely
- Meas. accuracy of CCD signal <30 e-
  - Noise: implement LPF & Correlated double sampling (CDS).
  - AD conversion : multi bitADC (over 5bit)



FPCCD2B prototype design 1

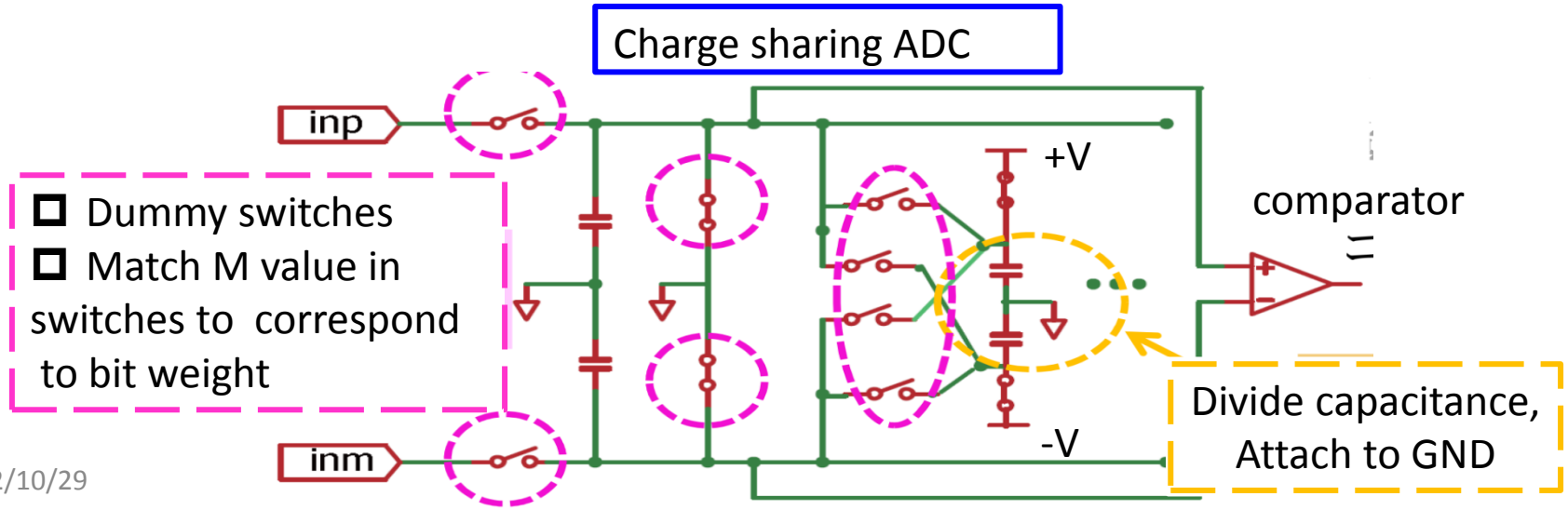
- FPCCD2B(2nd prototype ASIC)
  - For Readout speed and meas. accuracy requirements
  - 0.35umTSMC process, 8 ch
  - Chip size : 4.3mm × 4.3mm
- SAR ADC design
  - 8 bit signal
  - 8 consecutive capacitor blocks for charge sharing





FPCCD2B prototype design 2

- High speed and precision measurements
  - Suppress the effect of stray capacitance attached to switches and in between GND.
  - Increase current supply to ADC comparator by increasing # of pins 80→100

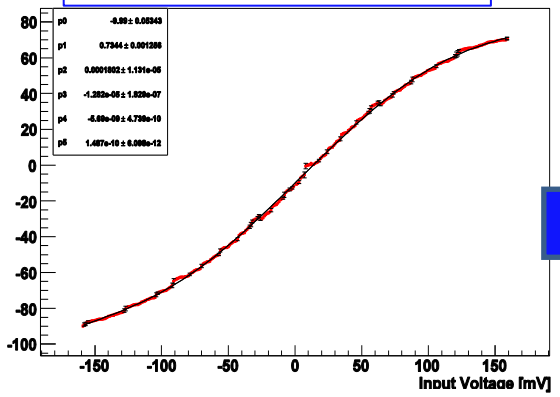


FPCCD2B results

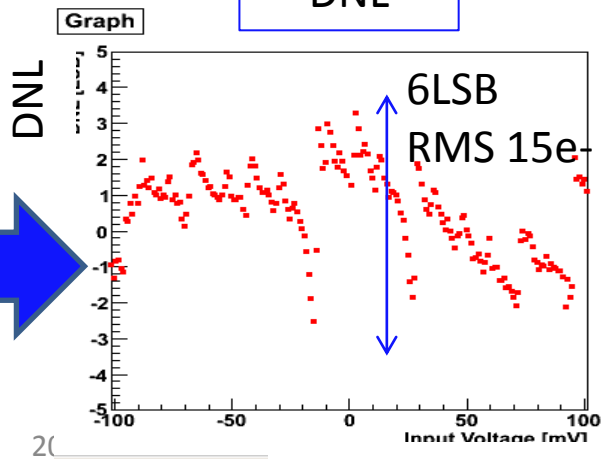
- Power consumption
  - 30.8mW/ch (>6mW/ch)→improved in next prototype
- $meas.accuracy = \sqrt{DNL^2 + pedestal\ width^2}$
  - $meas.accuracy@100MHzCK = \sim 16$ e-

＜30 e- required

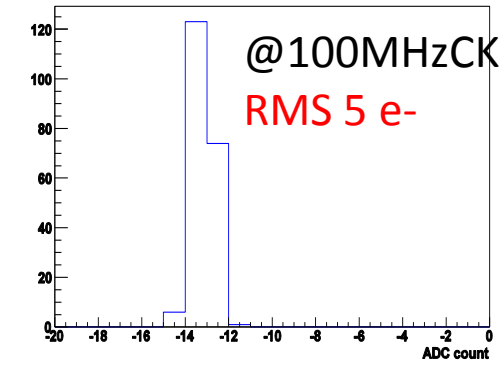
Input voltage vs ADC count



DNL



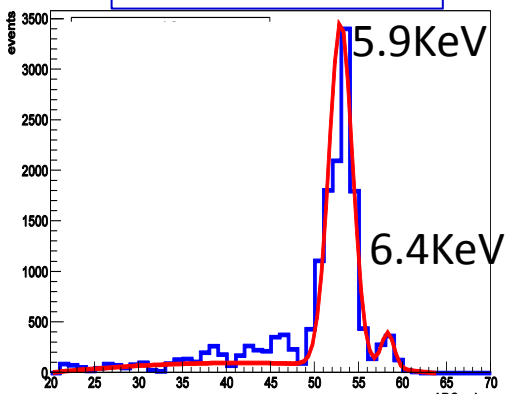
Pedestal distribution



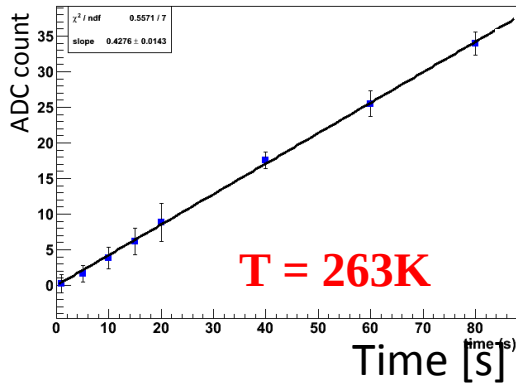
FPCCD2B results with CCD

- CCD(Manufactured by Hamamatsu Photonics)
  - 12x12um^2 two phase CCD
  - thickness : epi layer 15um, Si total 50um
- Fe55
  - irrad time10s,-40℃,3000 frames
  - S/N ： 37 (Single pixel hit ext)
  - energy resolution: 120 eV
- Pedestal analysis
  - Dark current suppressed under ILC conditions(200ms -40℃)
  - Noise ~55 e-
    (CCD readout main source)

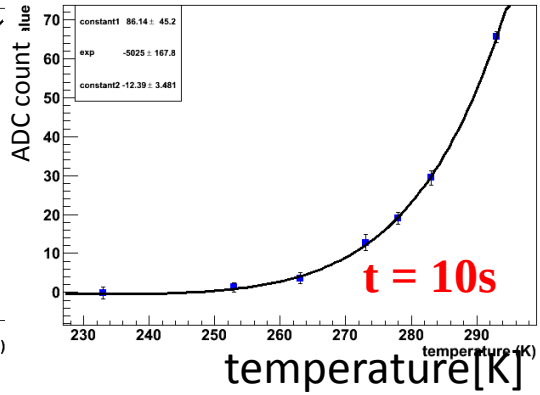
Fe55 spectrum



Time dependence



Temperature dependence

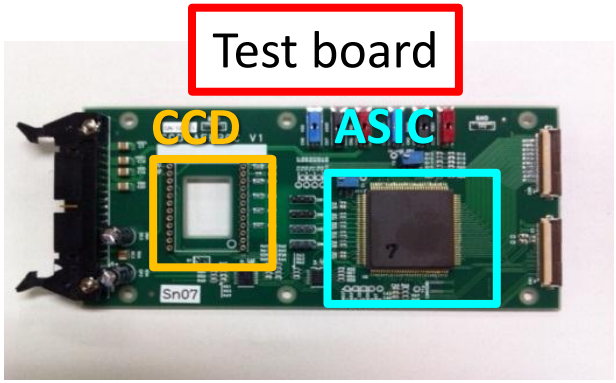


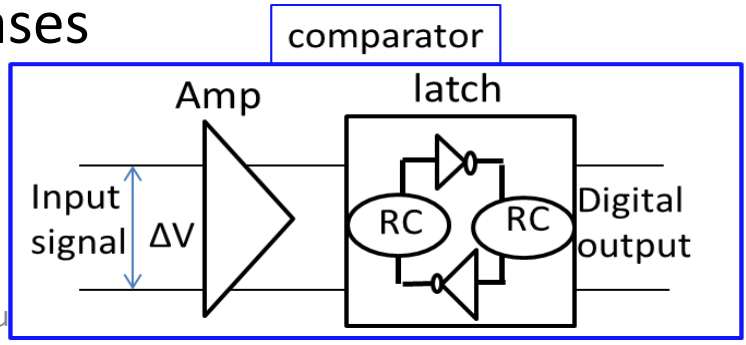
➢ FPCCD2B overall satisfies all requirements except power consumption

AFFROC01 design

- AFFROC01(3rd prototype ASIC)
  - Low power consuming prototype
  - TSMC CMOS process 0.25um
  - Chip parameter 3.7x3.75mm^2
- Power consumption modifications
  - Circuit simplification
  - Substitute with more energy conserving circuit
  - Process modification (0.35→0.25um)
- Modifications due to process modification
  - Comparator operation speed increases
  - Enable comparator speed control and improve DNL

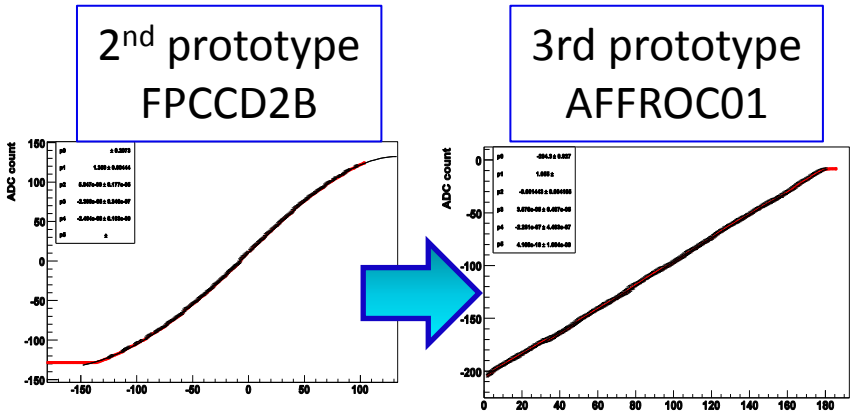
➢ Succeeded in 100MHz CK operation





AFFROC01 improvement results

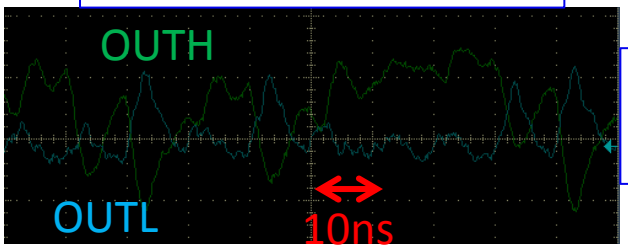
- INL(integral non linearity)
  - Shows curvature in linearity.
  - Caused upstream circuits.



INL 17% → < 2%

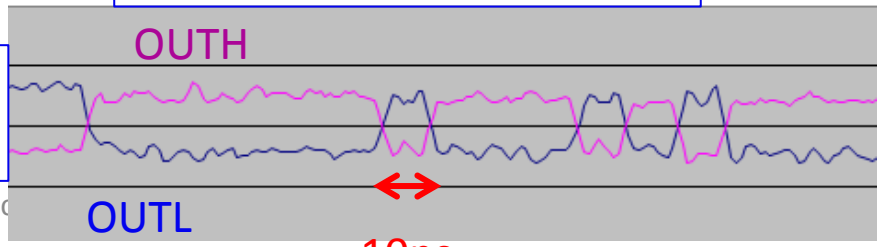
- baseband transmission
  - 10Mpix/s = 100MHz ADC comparator CK
  - Return zero→non return zero
  - Longer high period(10ns), Easy sampling

FPCCD2B : return zero



Measured LVDS output signal

AFFROC01: non return zero



AFFROC01 DNL improvement

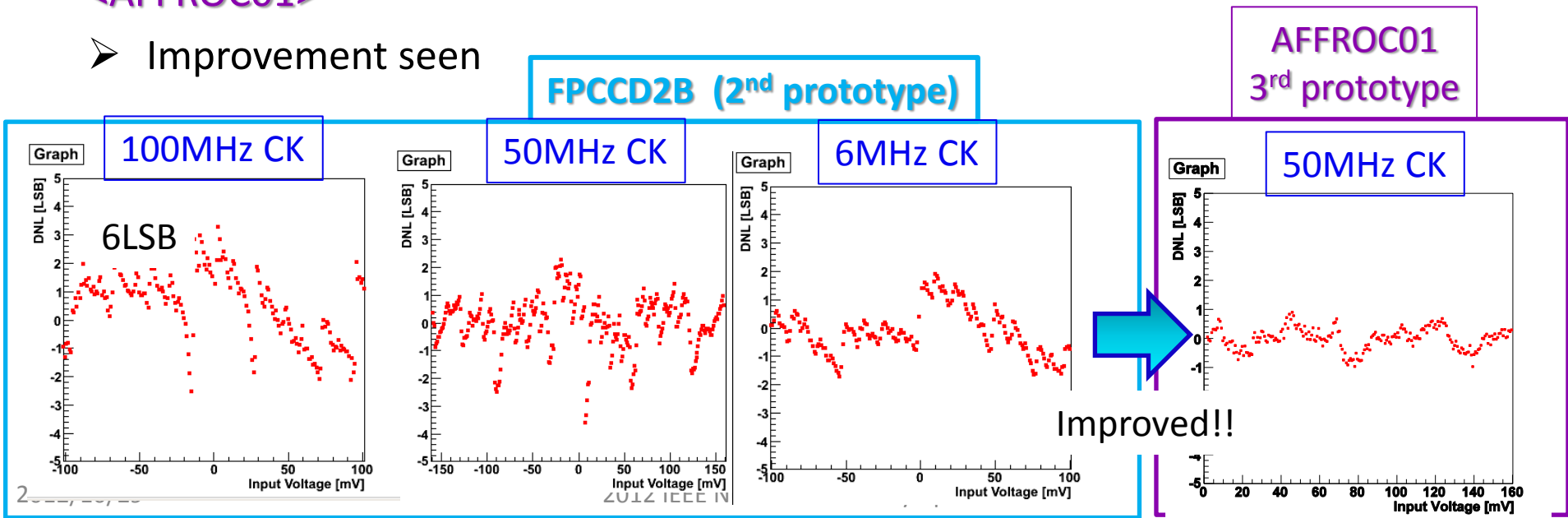
<FPCCD2B>

- DNL @ low frequency
  - capacitance ratio in SAR ADC capacitor displaced from bit weight
- DNL @ high frequency (100MHz CK)
  - meta-stable state @ bit change. Thus causes bit jump @high freq.

➢ Process change + Speed control @3rd prototype

<AFFROC01>

➢ Improvement seen



Summary

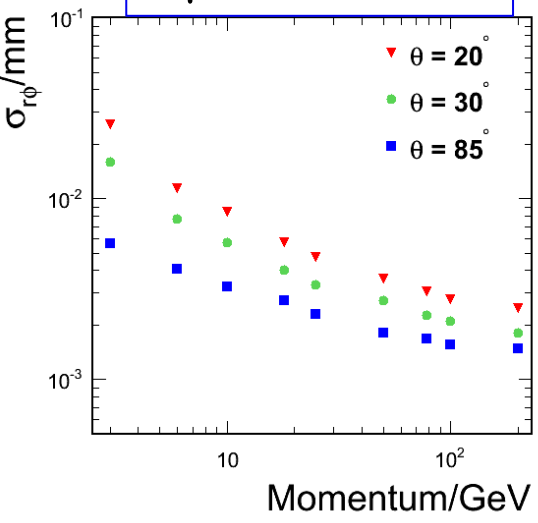
- FPCCD2B ASIC (2nd prototype)
  - Power consumption 30.8 mW/ch
  - Measurement accuracy 16 e- @100MHzCK
  - 55 e- when attached to 12um^2 CCD
  - Able to operate detailed CCD evaluation tests.
- ➢ FPCCD2B overall satisfies all requirements except for power consumption.
- AFFROC01 (3rd prototype) is working@100MHz CK
  - Improved Power consumption of 4.8mW/ch
  - As well as meas. accuracy and other improvements(INL, LVDS signal, DICEFF radiation tolerance)

BACKUP

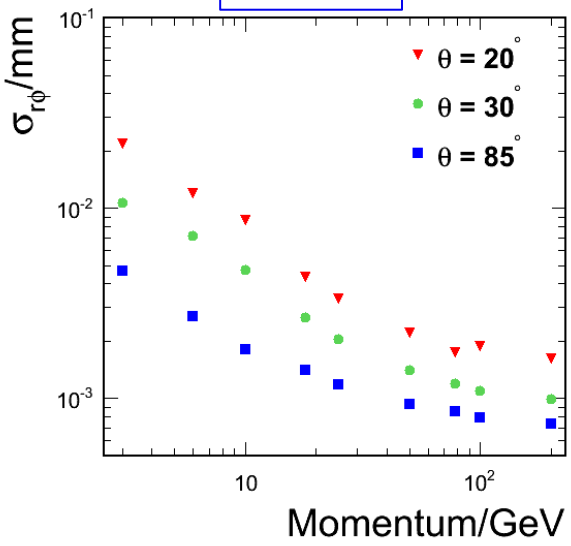
FPCCD impact parameter resolution & pixel occupancy

- FPCCD can improve the Impact Parameter resolution.
  - Significant improvement in high momentum region

3 μm resolution



FPCCD

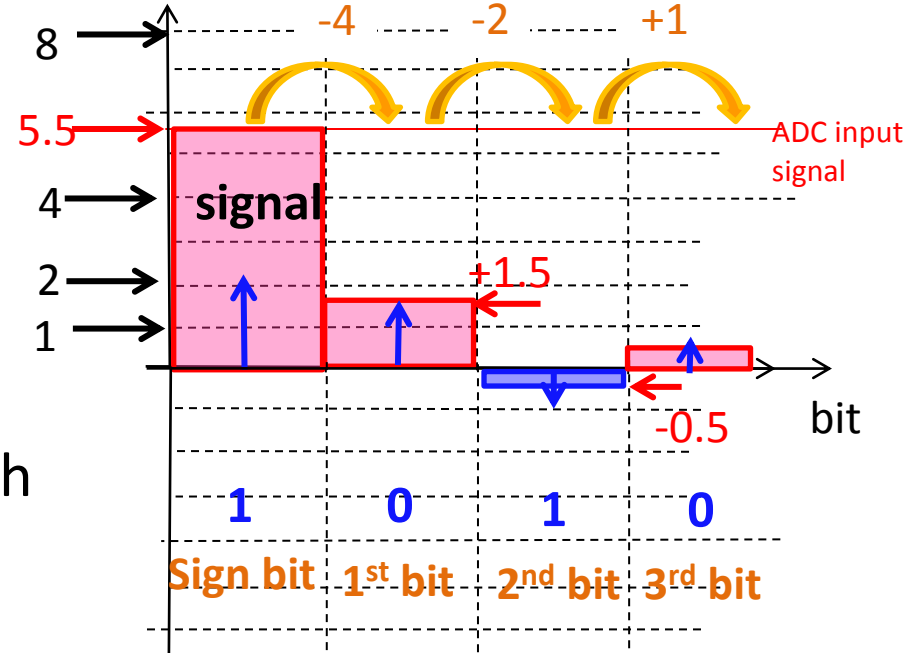


Pixel occupancy

Layer	500 GeV (sb2009wTF) [%]
1	3.1
2	1.7
3	0.09
4	0.07
5	0.017
6	0.015

Charge sharing ADC

- Charge sharing ADC
  - Compare standard 0 level & input charge(modified after determining every bit)
  - Determine to subtract or add stored charge(charge sharing)
  - There are 8 types of stored charge, each are binary weighted. (binary search)
- Low power consumption
  - SAR →one comparator
- High accuracy
  - Binary search
- Readout speed
  - Relatively high speed enough for requirement



FPCCD2B frequency dependence

- Detailed frequency dependency

  @ low frequency
  - SAR ADC capacitor, capacitance ratio displacement from bit weight

  @ high frequency (100MHz CK)
  - meta-stable state @ bit change. causes bit jump @high freq.