Development of readout ASIC for FPCCD vertex detector

2012.4.24 KILC12

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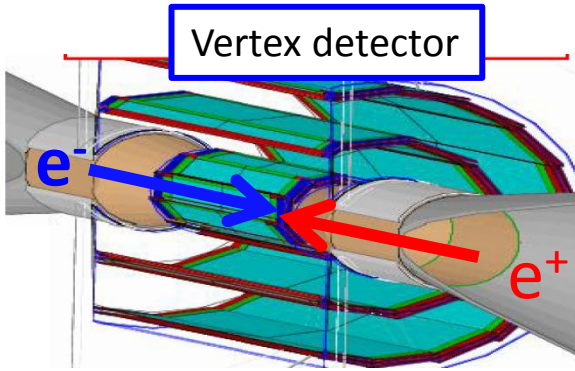
FPCCD Vertex detector

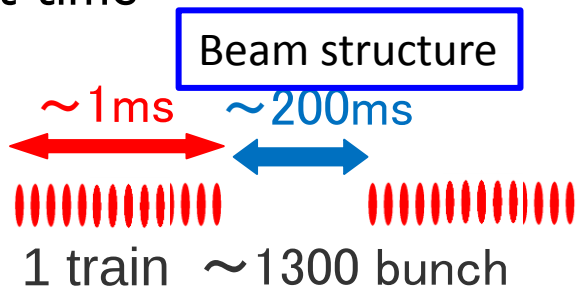
- Vertex detector
  - High vertex resolution ⇒ place detector near IP
  - Accurate track reconstruction ⇒ pixel occupancy~1%



➢ Finely segmented pixel.

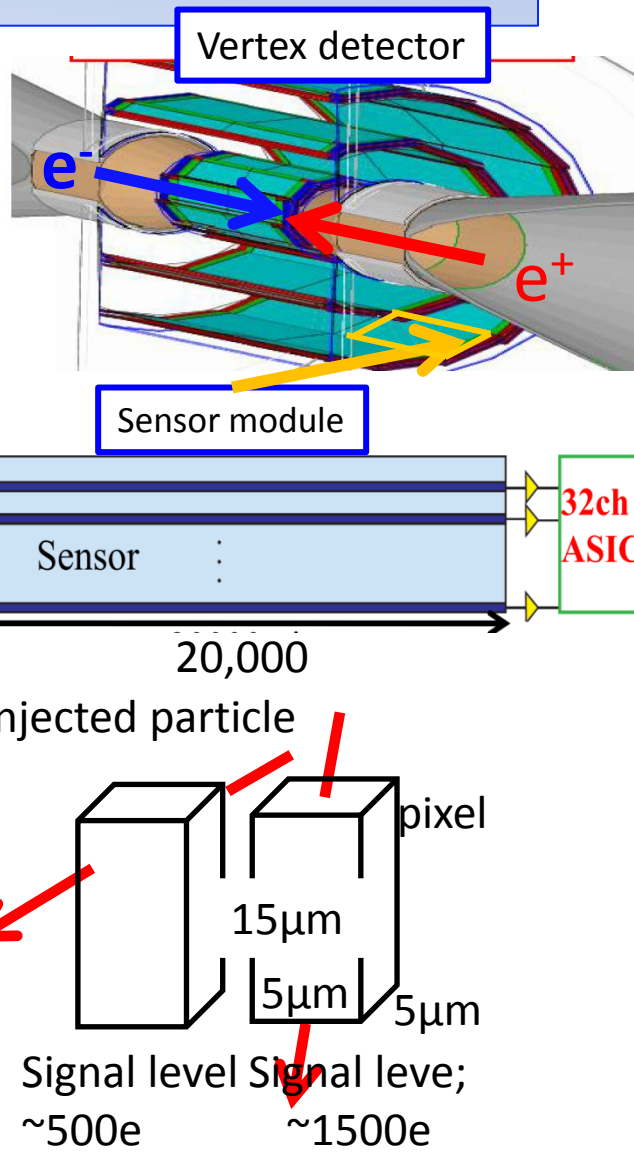
- FPCCD(FinePixelCCD) vertex detector
  - ☺ pixel size: $5 \times 5 \mu m^2$ ⇒ high resolution
  - ☺ depletion region:15μm ⇒ less multiple coulomb scattering
  - ☺ fully depleted ⇒ high 2 track separation capability
  - ☺ inter-train time readout ⇒ free from beam induced RF noise
  - ☹ total # of pixels : 1.6×10^{10} ⇒ long readout time

➢ Readout ASIC for FPCCD was developed



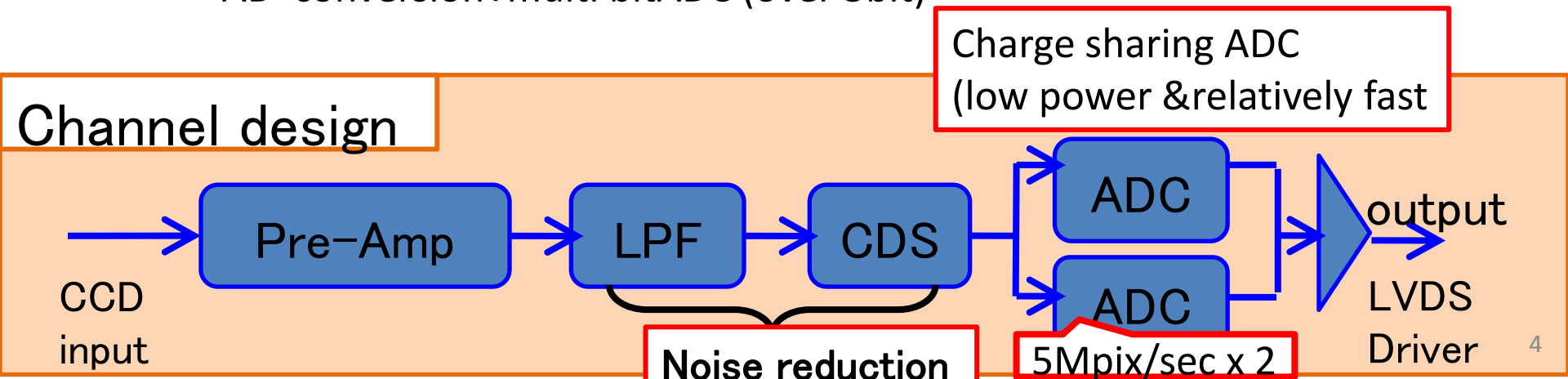
Requirements for FPCCD readout

- Power consumption < 6mW/ch
  - Placed in -40℃ cryostat.
  - Total power consumption<100W
- Readout speed> 10Mpix/sec
  - Readout Inter-train time(200ms)
  - 20,000x128pix/200ms
- Meas. accuracy of CCD signal < 30 e-
  - Small signal level : ~500e-
  - Noise level + ADC accuracy< 30e-



Measures for requirements

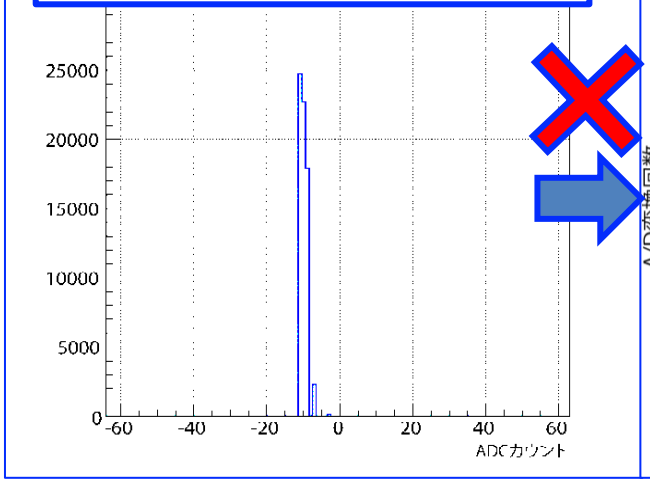
- Power consumption <6mW/ch
  - Main power source is ADC
  - Implement charge sharing ADC
- Readout speed>10 M pixel/s
  - Use two 5Mpixel/s parallely
- Meas. accuracy of CCD signal <30 e−
  - Noise: implement LPF & Correlated double sampling (CDS).
  - AD conversion : multi bitADC (over 5bit)



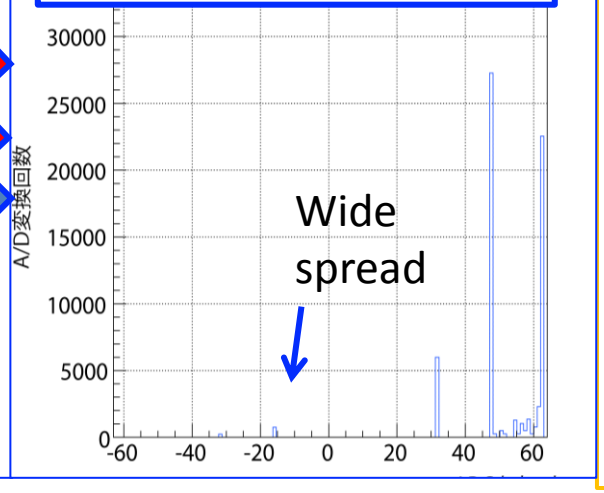
Problems in 1st prototype

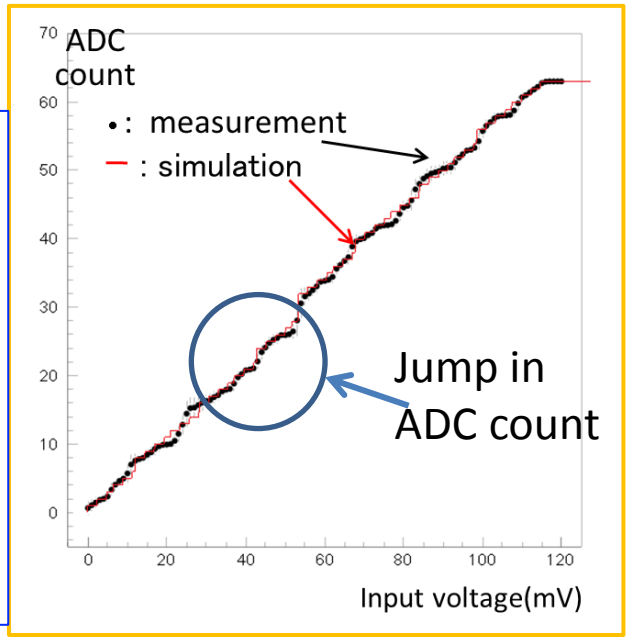
- Limitation of Readout speed (1.5Mpix/sec)
  - Possibility of current shortage to ADC comparator.
- Large jumps in ADC output
  - As an effect of stay capacitance, there is a possibility that capacitor ratio isn't corresponding to bit weight.

1.5Mpix/sec ADC output
Pedestal distribution



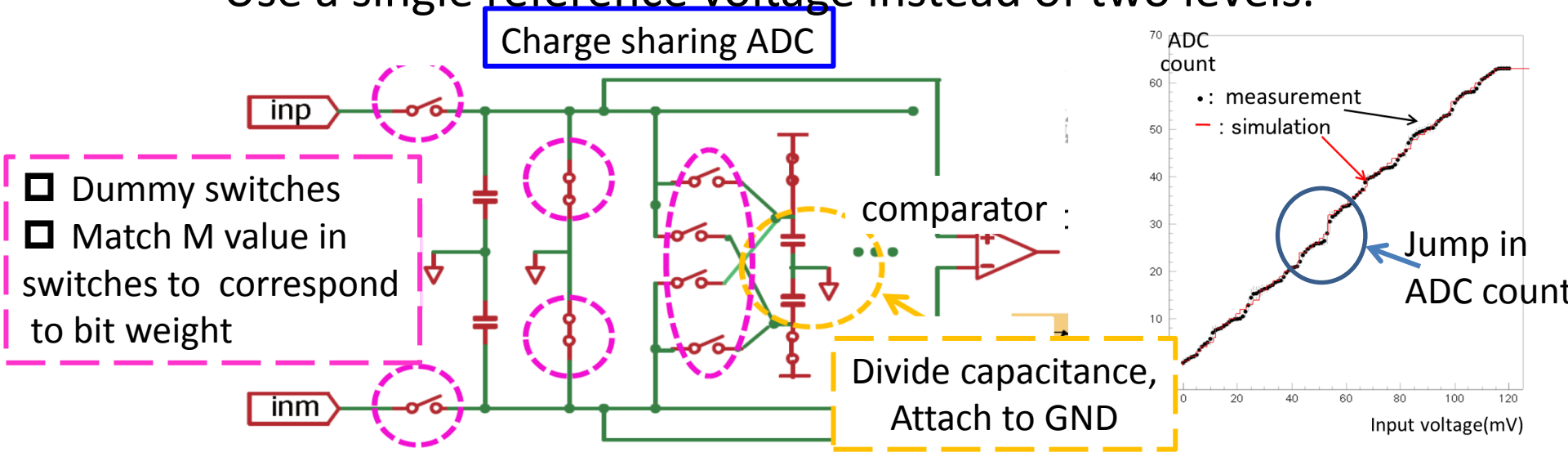
5Mpix/sec ADC output
Pedestal distribution





Measurements in 2nd prototype

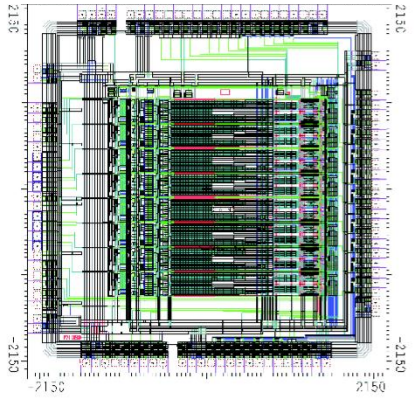
- Countermeasure against readout speed limitation:
  - Increase current supply to ADC comparator by increasing # of pins 80→100
- Countermeasure against jumps in ADC count:
  - Suppress the effect of stray capacitance attached to switches and in between GND.
  - Use a single reference voltage instead of two levels.

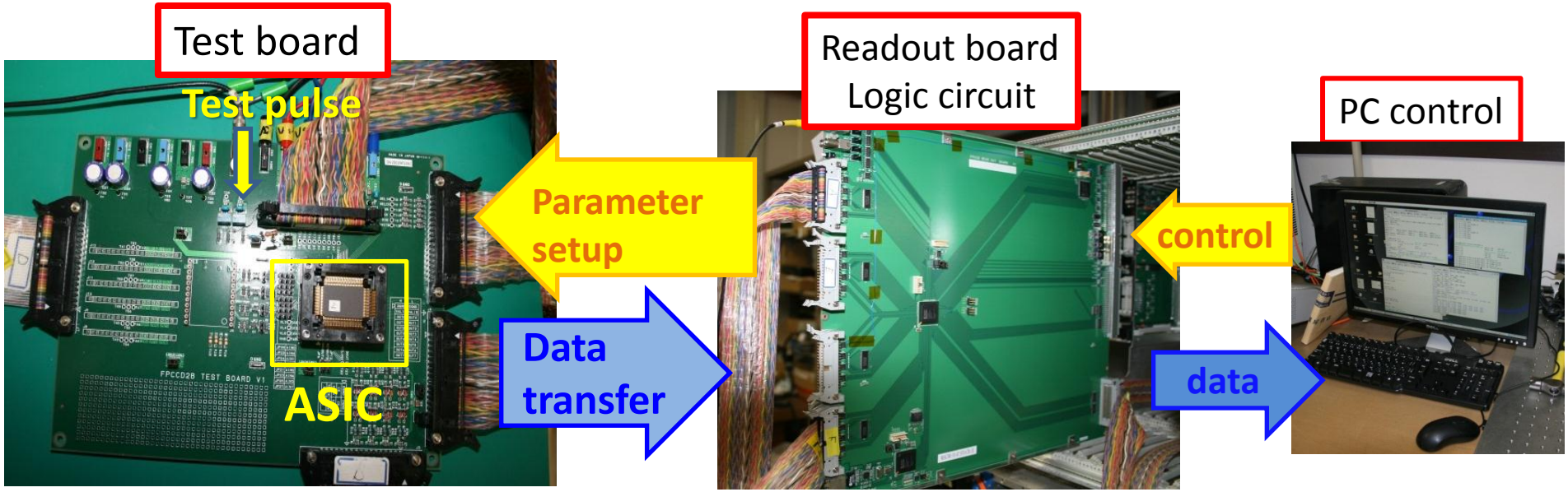


2nd prototype and test bench

- 2nd prototype of readout ASIC
  - 0.35umTSMC process
  - # of channels : 8 ch
  - Chip size : 4.3mm × 4.3mm
  - 8 bit signal(100MHz CK)

2nd prototype layout

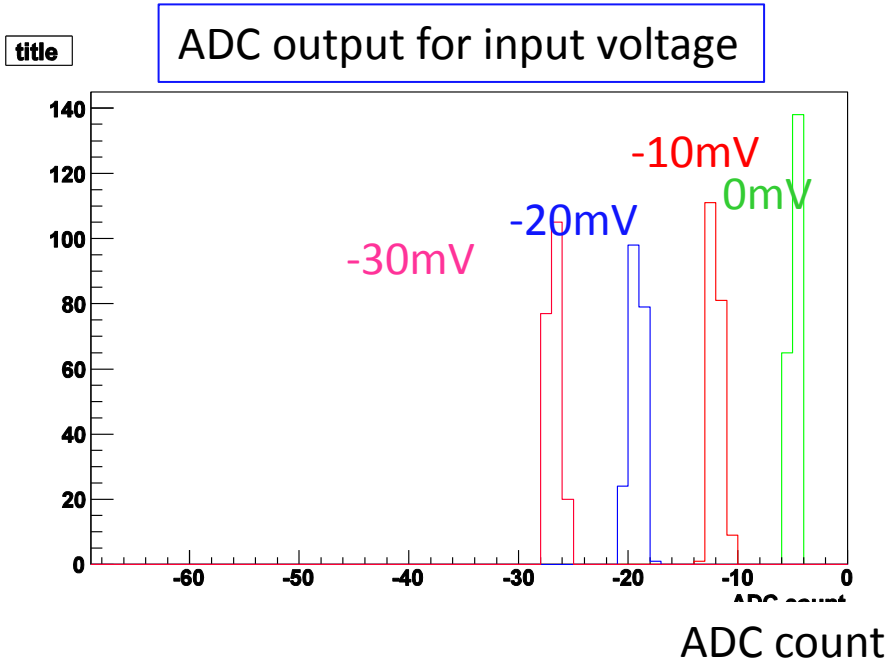




Results of 2nd prototype: readout speed

- ADC output @100MHz CK
  - ADC output has a single output for a curtain input voltage.

➢ Success in 100MHz readout



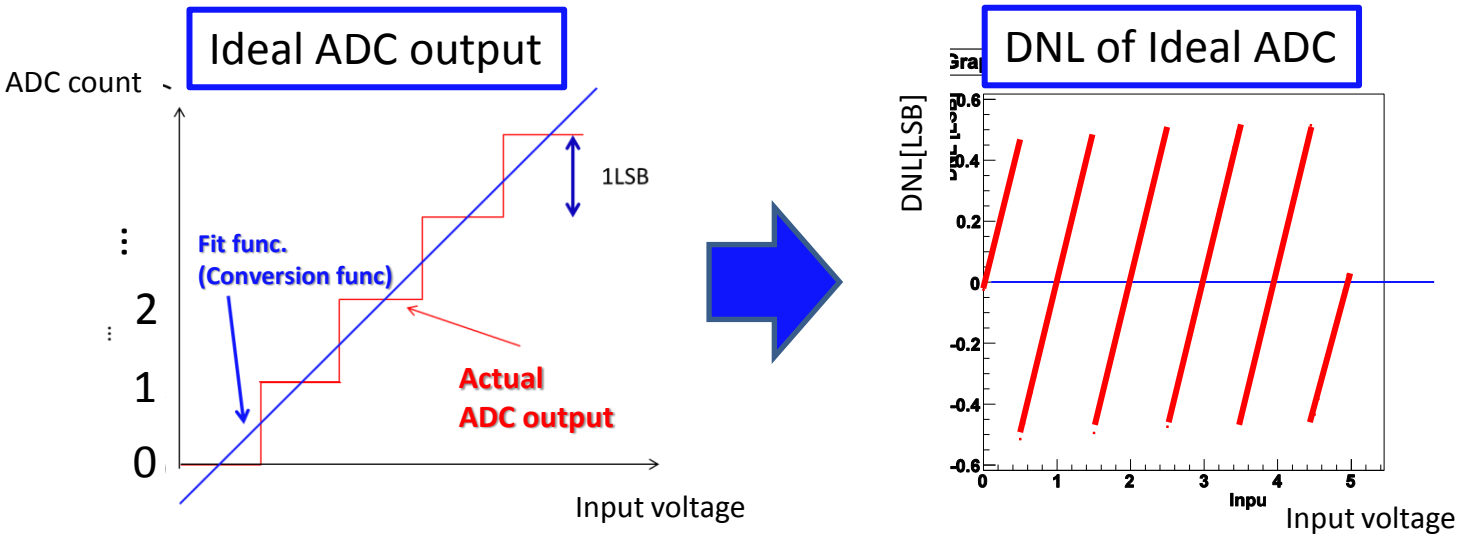
Readout accuracy

■ Differential non linearity(DNL)

$$DNL \equiv f(x) - data(x)$$

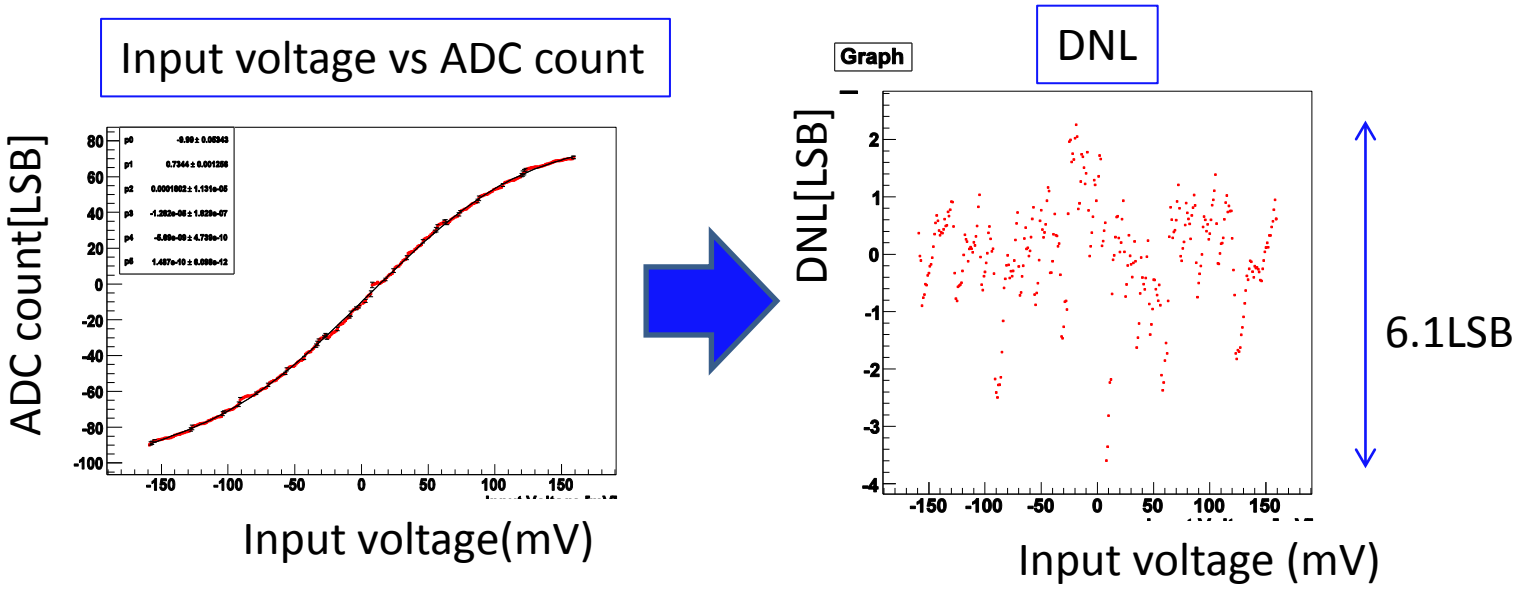
x: input voltage
f(x): $fit\ function\ (conversion\ function)$
$data(x)$: $ADC\ output\ for\ inputvoltage$

➢ Evaluate conversion accuracy of ADC from DNL.



Results of 2nd prototype: Conversion accuracy

- Differential non linearity(DNL)



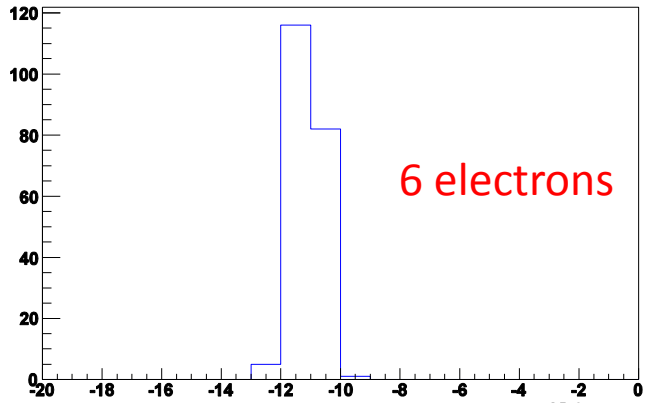
$$convesion\ acc. = \frac{6.1[LSB]}{\sqrt{12}} = 1.8\ [LSB] \quad (15\ electron)$$

Results of 2nd prototype: Meas. Accuracy of input signal

- Extract noise level from Pedestal distribution of ASIC. (@100 MHz CK)
  - Room temp: 6 electrons , low temp(-40℃): 5 electrons

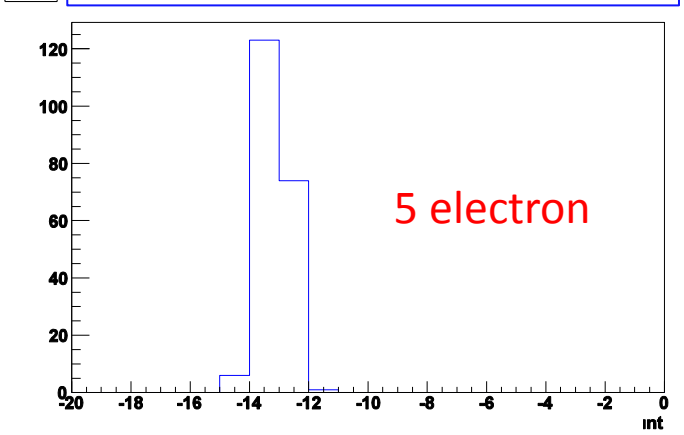
$meas.accuracy = \sqrt{conv.acc.^2 + noise^2} = 16$ elcetrons **＜30 electrons: requirement**

Pedestal distribution @ room temp



ADCcount

Pedestal distribution @-40℃



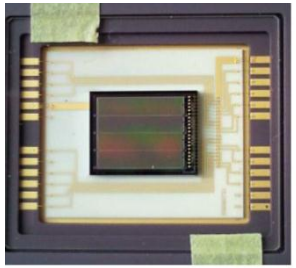
ADC count

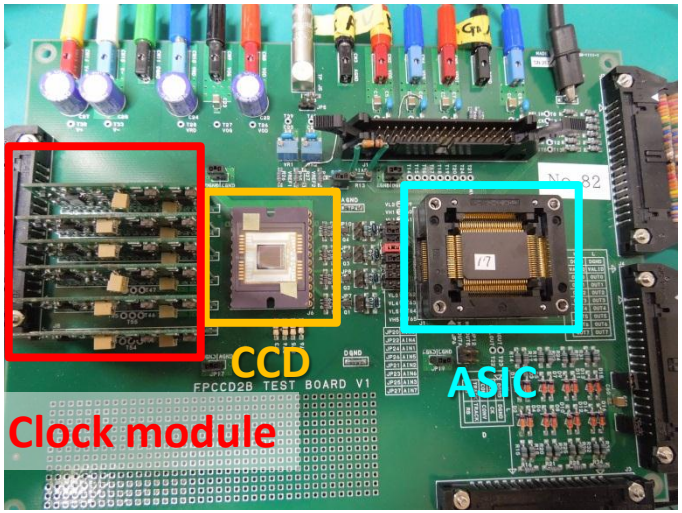
FPCCD READOUT WITH 2ND PROTOTYPE ASIC

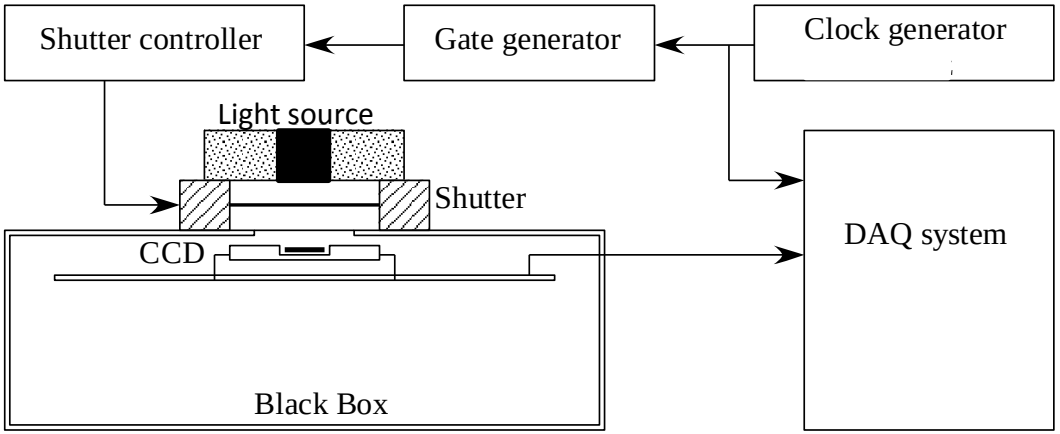
FPCCD readout

- FPCCD sensor prototype
  - Manufactured by Hamamatsu Photonics.
  - Pixel size ： 12um × 12um
  - Number of channel ： 4 ch
- Test bench

FPCCD sensor prototype



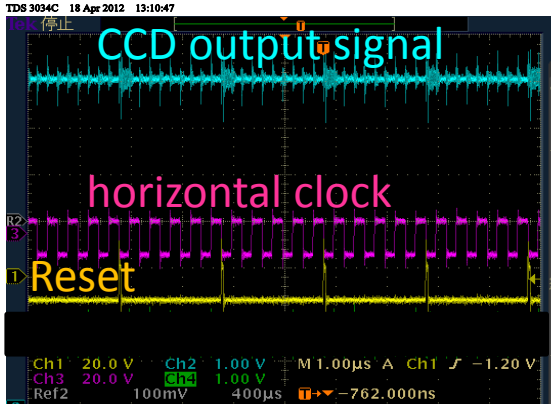




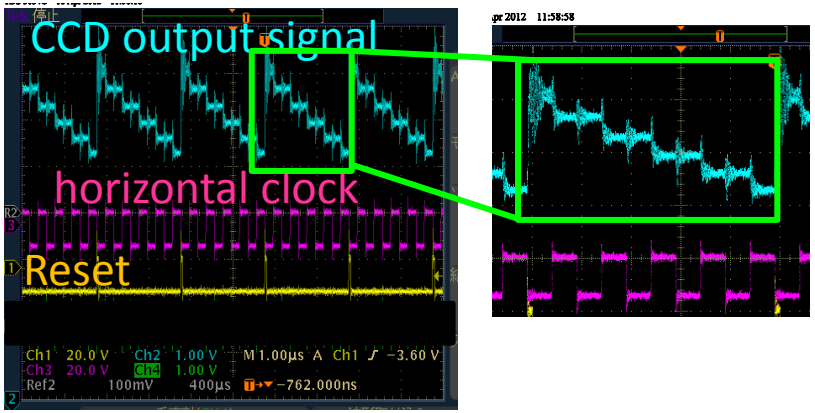
FPCCD output

- Check output of FPCCD test sample(@2.5Mpixel/s)
  - Reset every 5pixels to check the CCD operation

No light



light

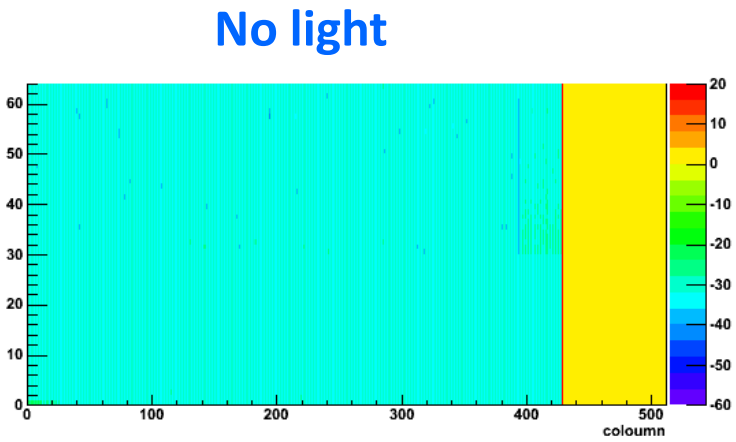


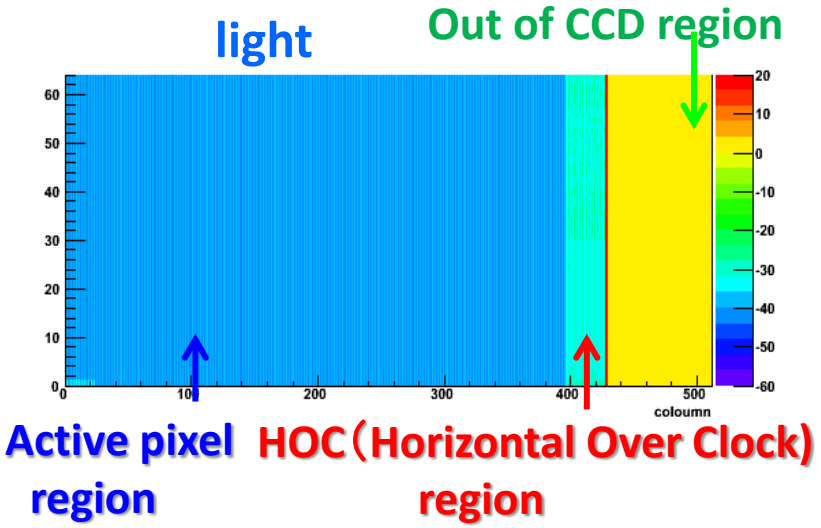
➢ **The output signal can be observed from the FPCCD .**

FPCCD Readout

- LED irradiation to FPCCD test-sample
  - No reaction to light at HOC(Horizontal Over Clock) region
  - Reaction to light at active pixel region

➢ Success in developing a FPCCD readout system.





3RD PROTOTYPE

2nd prototype power consumption

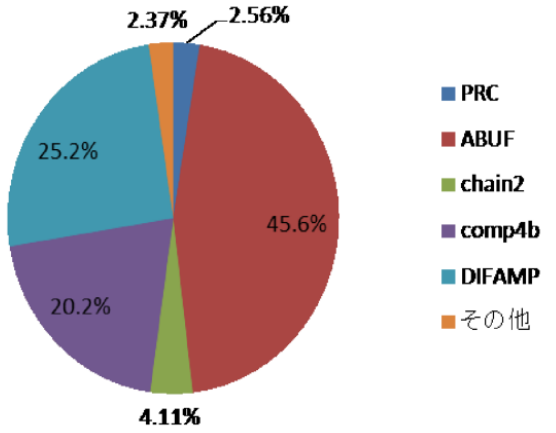
- 2nd prototype power consumption

Measured power consumption

Digital power	Analog power	Total Power	requirement
12.5[mW/ch]	18.4[mW/ch]	30.9[mW/ch]	6[mW/ch]

- Analog power consumption meas.
  - Enable to turn off monitor circuit.
  - Take out Diffamp→improve dynamic range, INL.
  - Turn off comp CK when not used.

Analog Power consumption and circuits



3rd prototype power consumption measurements

- Digital power consumption
  - Stop DC current in I/O Buffer when ASIC is running (10% reduction)
  - Take out sequencer (ADC bit shift register) & place in TOP level.
- Total power consumption
  - Change Process 0.35µm→0.25µm

power consumption improvements and side effects

- 3rd prototype power consumption result

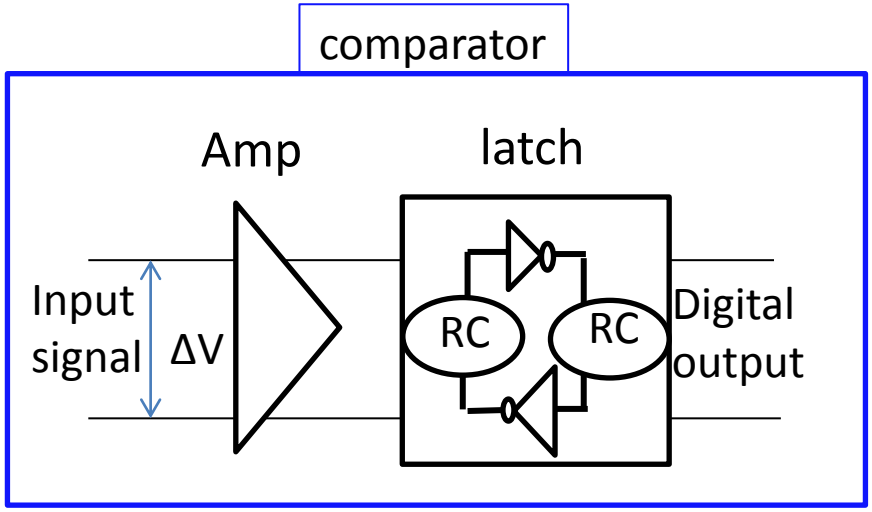
Meas. Power consumption simulation result

Digital power	Analog power	Total power	Requirement
3.8[mW/ch]	1.6[mW/ch]	5.4[mW/ch]	6[mW/ch]

- ➢ 5.4mW/ch power consumption. Requirement clear
- Merit of process change(0.35µm→0.25µm)
  - Reduction of power voltage
  - Reduction of Transistor capacitance.
- ➢ Power reduction
- demerits of process change(0.35µm→0.25µm)
- ➢ DNL degradation due to comparator speed increase.
- ➢ Radiation tolerance towards SEE(Single Event Effect) is weakened.

Comp operation speed & DNL

- Comparator speed control
  - Comp. is composed of a amp and a latch.
  - Increase in operation speed causes amplified level to become unstable.
  - ➢ Adjust time constant and prevent malfunction of comp.

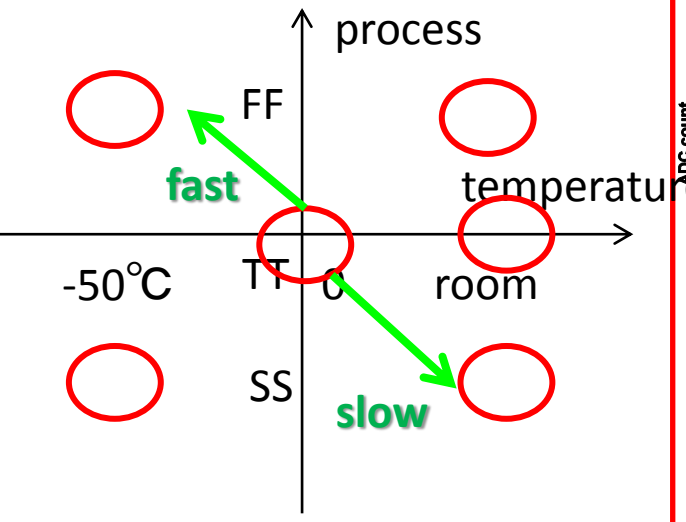


Speed related parameter & DNL

- Speed related parameters
  - Process dispersion, temperature

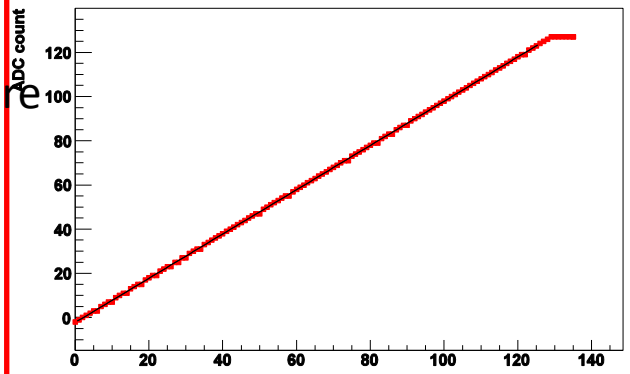
➢ DNL is suppressed within ±1[LSB].

Speed related parameters & DNL



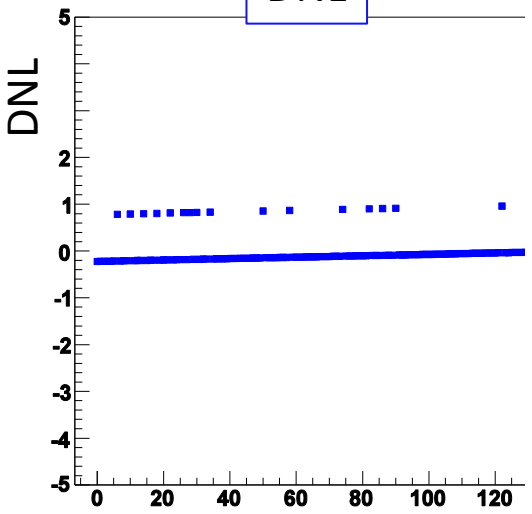
Post layout simulation

linearity



CCD input voltage (mV)

DNL



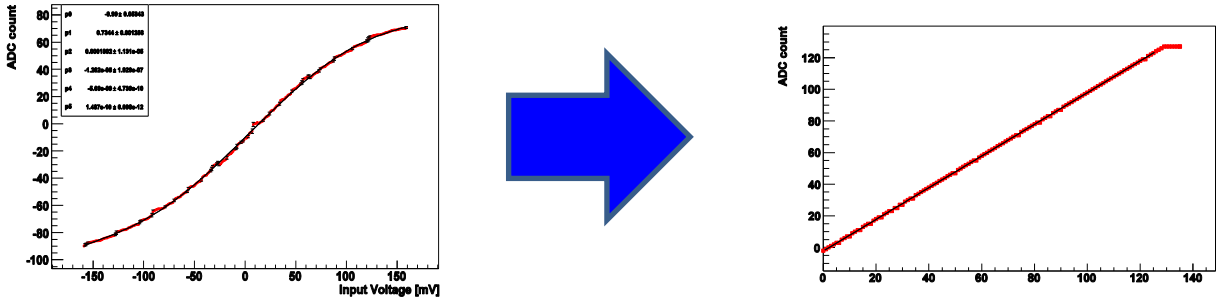
CCD input voltage (mV)

Other improvements

- Linearity

<Integral Non Linearity(INL)>

  - 2nd prototype: 17.1%→3rd prototype: 0.380%

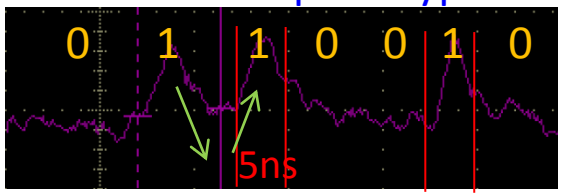


- Radiation damage
  - DICE FF: radiation hardened by design flip-flop with high single event effect(SEE) immunity.
  - Heavy ion testing →beam test

Other improvements

- Reduction of wiring
  - Generate operational signals within ASIC.(from CK and SYNC.)
- Digital transmission system for output signal
  - RZ: 100MHz=period 10ns ∴pulse width Max:5ns
  - shaped like an triangle →400MHz sampling necessary.
  - NRZ:100MHz=period 10ns , pulse width Max 10ns

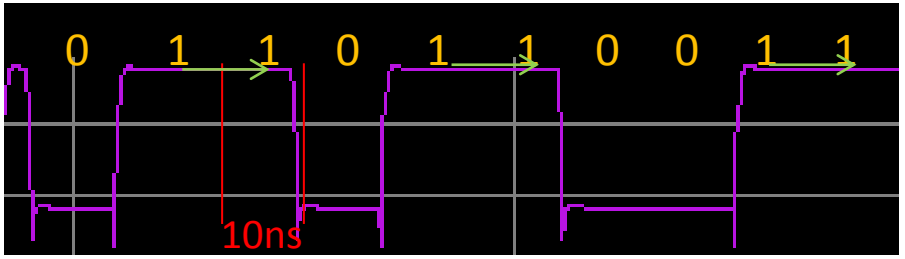
Result of 2nd prototype



RZ (Return-Zero) ⟷ 10ns

Short High period＝can easily mis-sample

Simulation result of 3rd prototype



NRZ (Non-Return-Zero)

Change to NRZ
＋return ADC CK signal for synchronization

Summary and plan

<SUMMARY>

- Evaluation of 2nd prototype ASIC
  - Meet all requirements except power consumption
- Developed FPCCD readout system for the 2nd prototype ASIC.
- Post layout simulation of 3rd prototype
  - Meet all requirements
  - Additional improvements: linearity, radiation tolerance, digital transmission system, reduction in # of wires for ASIC operation.

<PLAN>

- 2nd prototype
  - Radiation test using Fe55 & Sr90
- 3rd prototype
  - Service shuttle : May~ June tape out
  - Chip arrival: ~Oct.

3rd prototype layout