Readout ASIC of Pair-monitor for ILC

H.Ikeda [A], K.Ito [B], A.Miyamoto [C], T.Nagamine [B], R.Sasaki [B],
Y.Sato [B], Y.Takubo [B], T.Tauchi [C], H.Yamamoto [B]

A : JAXA, B: Tohoku University, C : KEK

Presented by Yutaro Sato

Tohoku university

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Outline

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   - Pair-monitor
2. **Development of the readout ASIC**
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   - Operation test
3. **Pair-monitor with SOI technology**
4. **Summary**

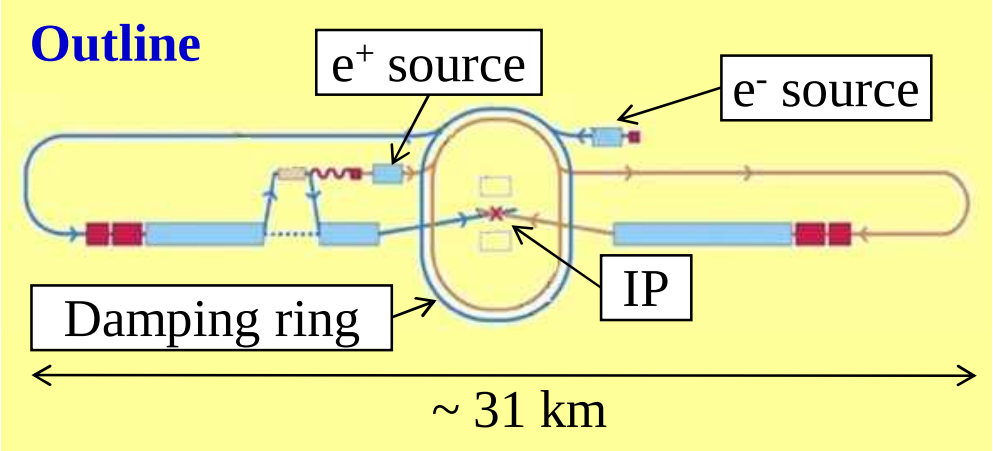
1. Introduction

International Linear Collider

ILC (International Linear Collider)

Next generation of the high-energy $e^+ e^-$ collider

- Purpose
  - Study Higgs, new physics …



- Parameters
  - CM energy : 500 GeV (upgrade to 1 TeV)
  - Integrated luminosity : $2 \times 10^{34}\ cm^{-2}\ s^{-1}$

→ Beam profile monitor is necessary to keep the high luminosity.

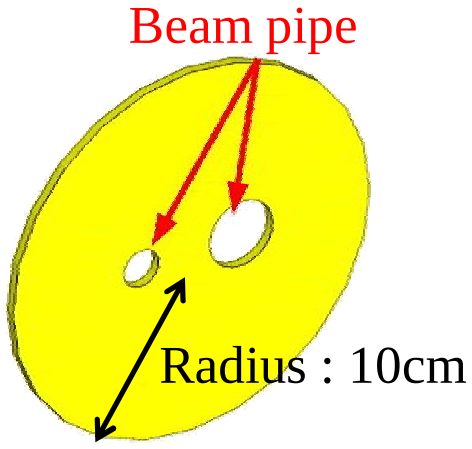
Pair-monitor

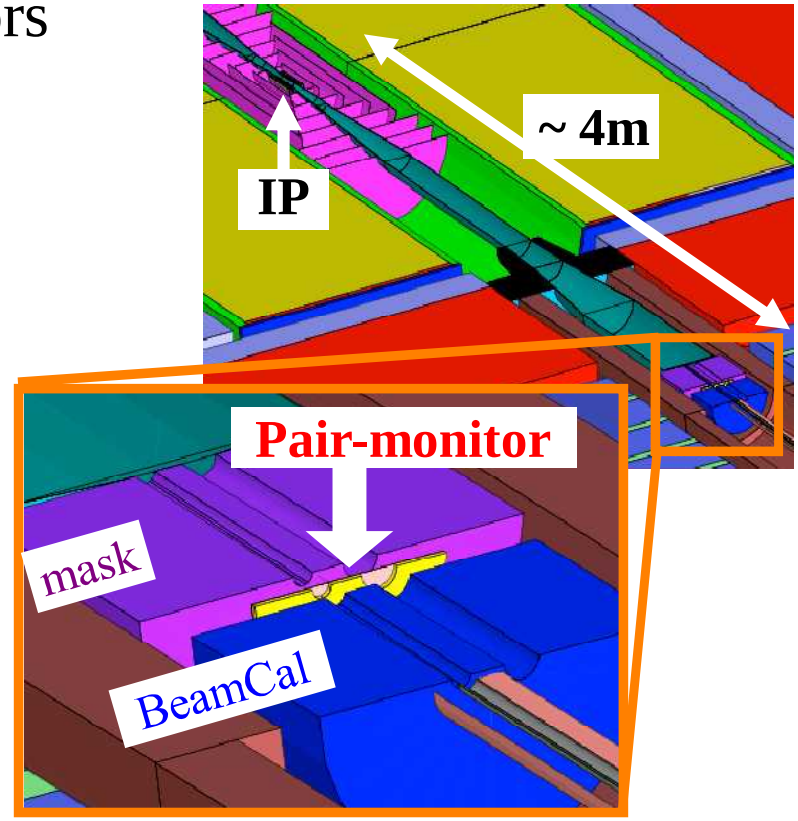
Requirement to the beam profile monitor

- Measurement accuracy of the beam size : < ~10 %
  - Beam size : (σ_x, σ_y, σ_z) = (639nm, 5.7nm, 300μm)
- Quick feed-back of measurement result
- No disturbance of other particle detectors

→ Candidate : Pair-monitor

- Silicon pixel sensor
- Location : ~4m from IP
- Radius : 10cm



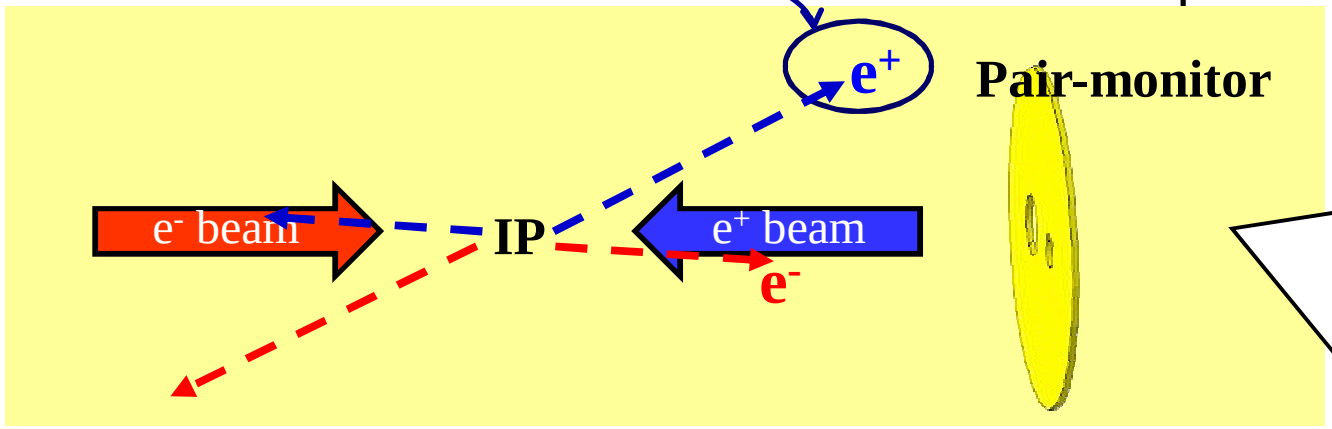


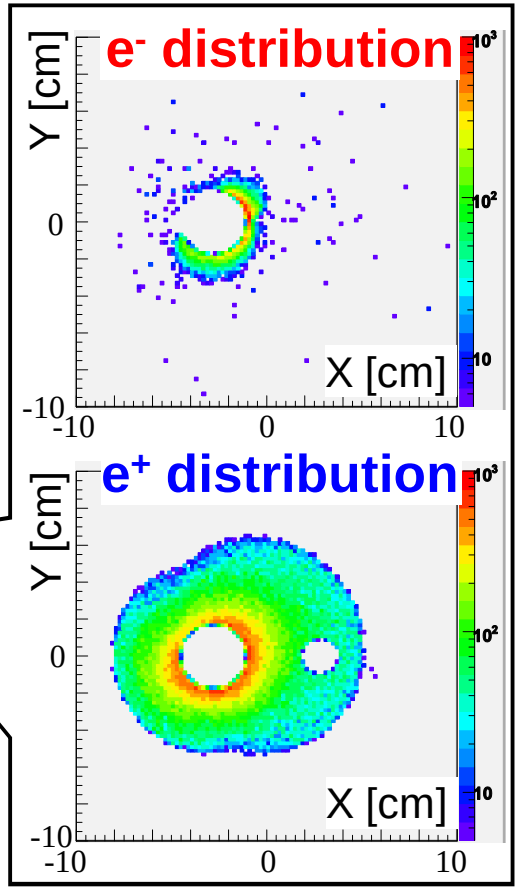
Beam profile measurement

Idea of the beam profile measurement

Pair-monitor measures σ_x and σ_y of the beam at IP, using the hit distribution of the pair B.G.

- A lot of the pair B.G are created during beam crossing.
- The same charges with respect to the oncoming beam are scattered with large angle.
- The scattered particles have information on beam shape.





→ Tohoku group has developed the pair-monitor.

2. Development of readout ASIC

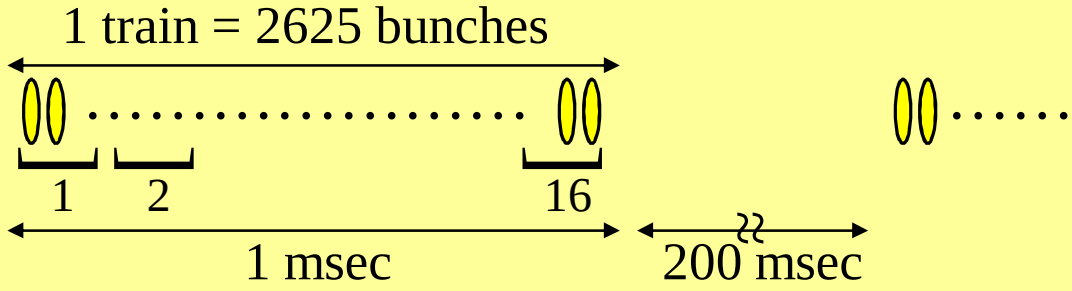
Development of the readout ASIC

As the first step, readout ASIC was developed.

Design concept of readout ASIC

- Pair-monitor measures the hit distribution of the pair B.G.
- Measurement is done for 16 parts in one train
  for the time-dependent measurement.
  - 16 Hit counts are stored at each part.
  - Count rate : < 2.5 MHz / (400μm x 400μm)
  - Information of the energy deposit is not necessary.
- Data is read out during inter-train gaps. (~ 200 msec)

Beam structure at ILC



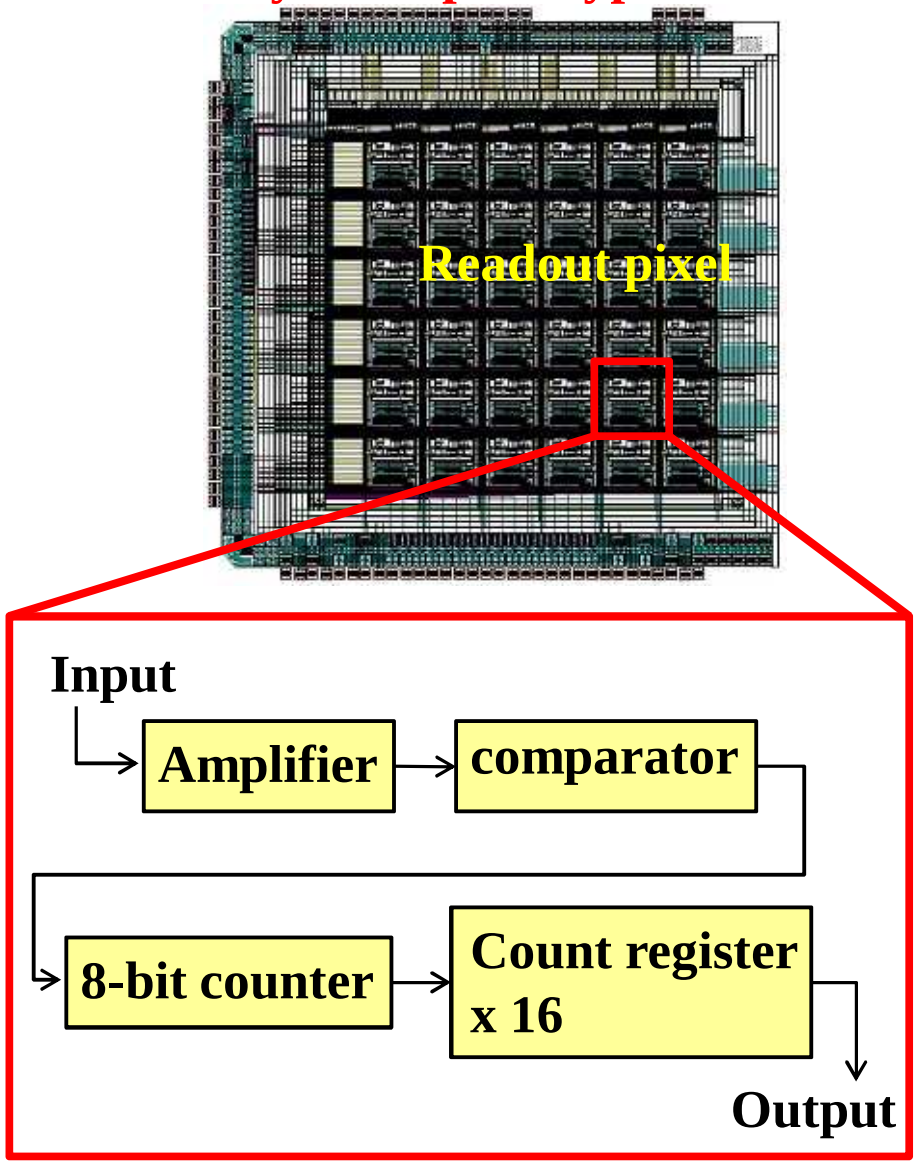
→ The prototype readout ASIC was designed to satisfy these concepts.

Design of readout ASIC

Design of readout ASIC

- 36 (6 x 6) readout pixels
  - Amplifier
  - comparator
  - 8-bit counter
    - ➢ to hit a number of hits
  - 16 count-registers
    - ➢ to store hit counts
- Shift register
  - ➢ to select a pixel from 36 pixels

Layout of prototype ASIC

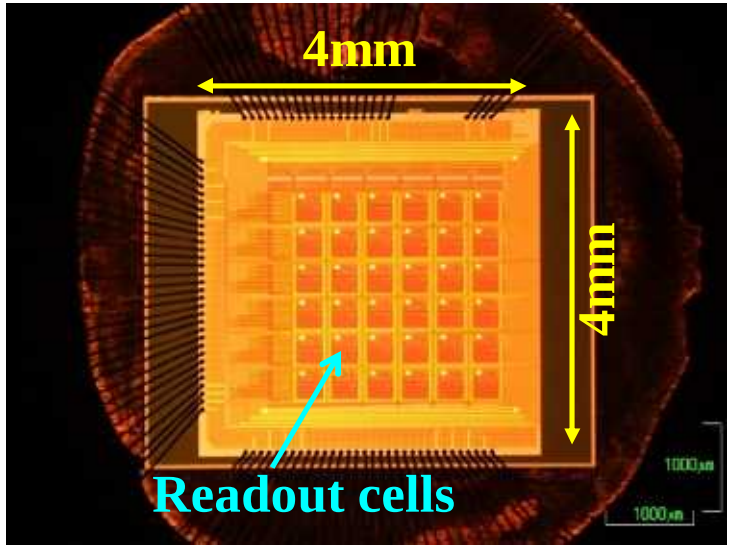


Prototype of Readout ASIC

The prototype of the readout ASIC was developed.

Prototype ASIC

- Production process : 0.25 μm TSMC
- Chip size: 4 x 4mm^2
- # of pixel : 36 (= 6x6)
- Pixel size : 400 x 400 μm^2
- Sensor will be bump-bonded to the ASIC.
- The chip was packaged in a PGA144.



→ The 3rd production of the readout ASIC was done in Oct. 2008.

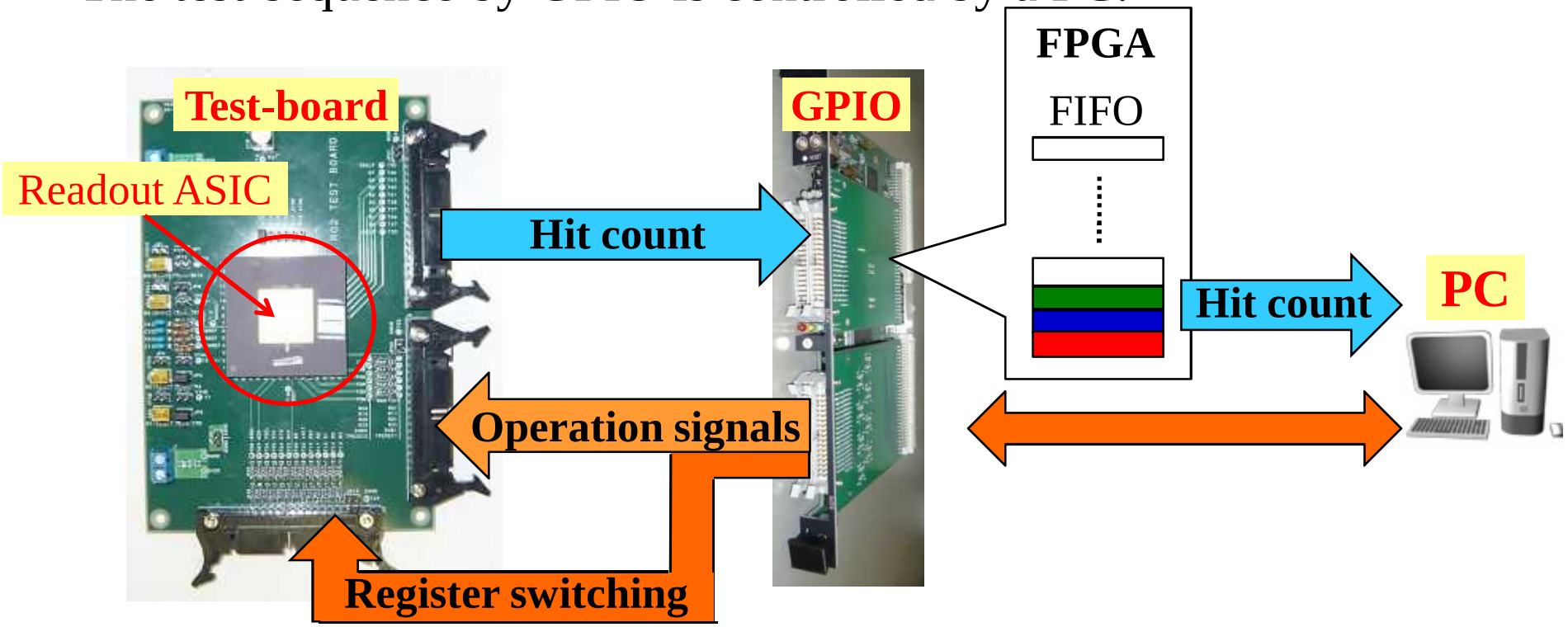
→ The trouble was found in the 1st and 2nd production.

Test system

The operation test was performed.

Test system

- GNV-250 module was used for the operation and readout .
  - KEK-VME 6U module
- The test-sequence by GPIO is controlled by a PC.



Problem in the 1st production (1)

The 1st production of the readout ASIC was done in 2006.

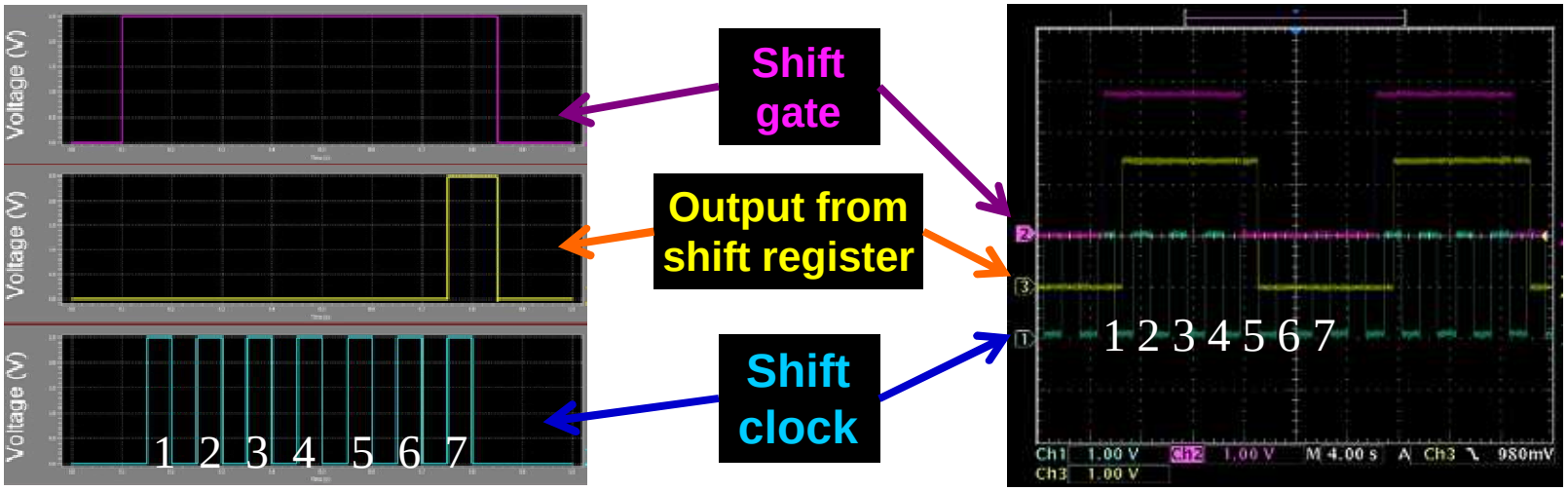
Problem

- The shift register to select a readout pixel did not work correctly.
  - The readout pixel is selected by the number of the shift clock.

Shift clock → x_1 → x_2 → x_3 → x_4 → x_5 → x_6 → Output

  - Output should rise at 7th clock, and fall when the shift gate falls.

Simulation **Measurement**



→ The reason of the problem was investigated.

Problem in the 1st production (2)

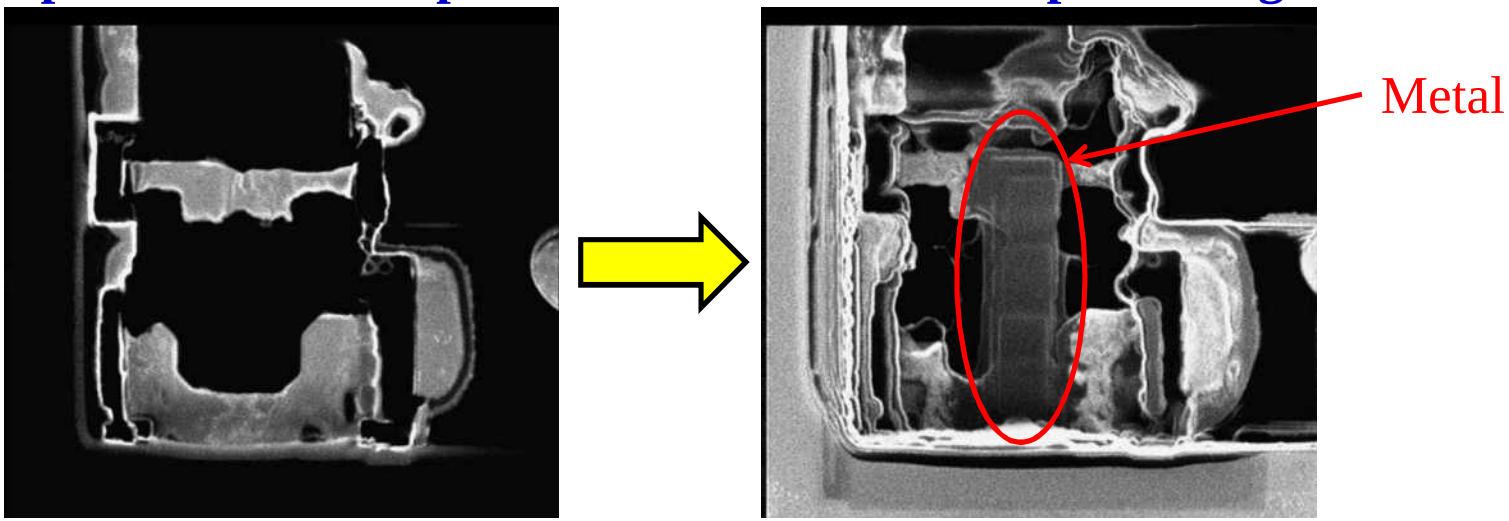
Reason

- The input register had disconnection.
  - The layout information is not defined in the process library.

The disconnected input line was connected

with FIB (Focused Ion Beam) processing . (@VDEC sub-center of Osaka Univ.)

Exposed location of problem **After FIB processing**



- After FIB processing, the shift register worked correctly.

→ The 2nd production was done with the input registers removed.

Problem in the 2nd production

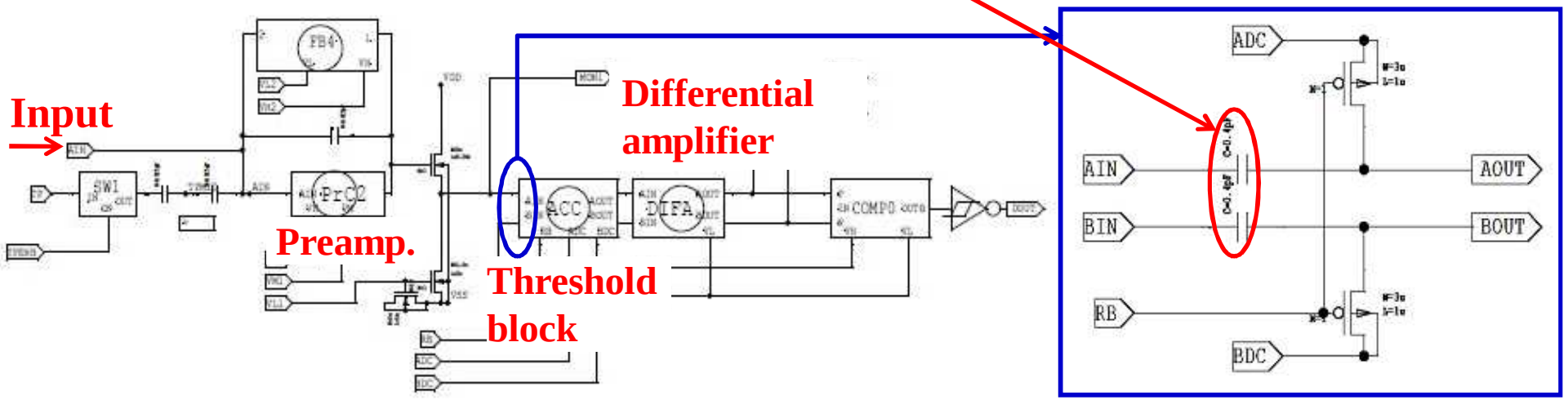
The 2nd production of the readout ASIC was done in 2007.

Problem

- The signal did not pass between pre-amplifier and threshold block.

Reason

- The layout mask for the MIM capacitor was missing due to a mistake.

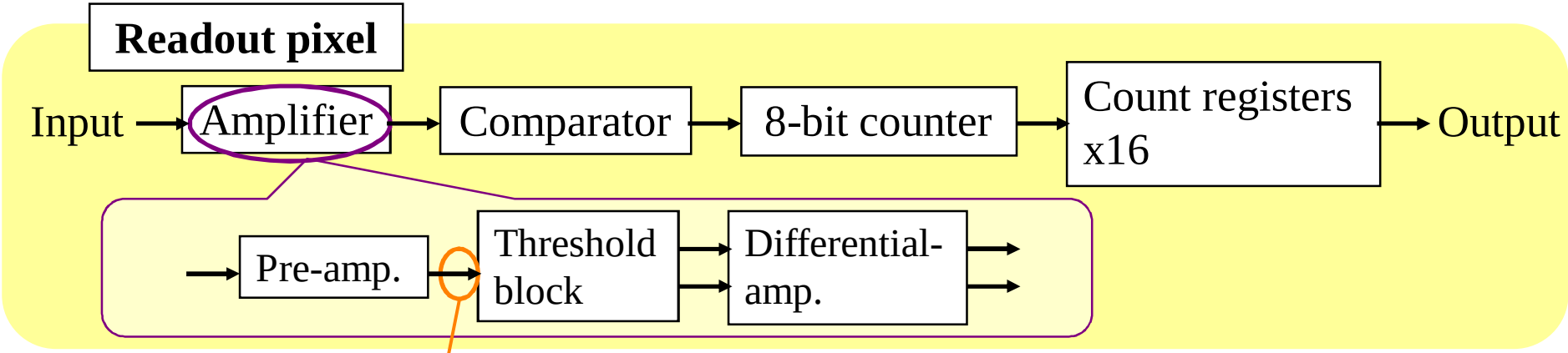


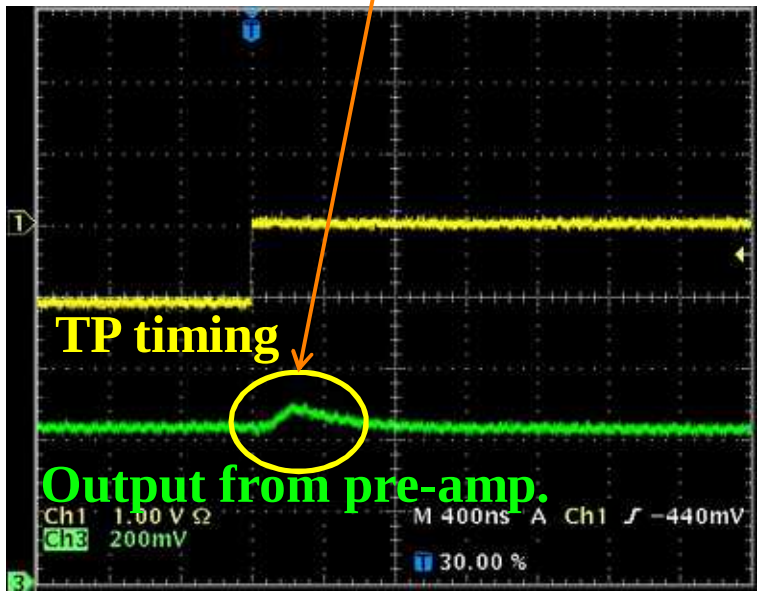
→ The 3rd production of the modified readout ASIC was done.

Response of pre-amplifier

Operation test of the 3rd production

The response of the pre-amplifier was checked.



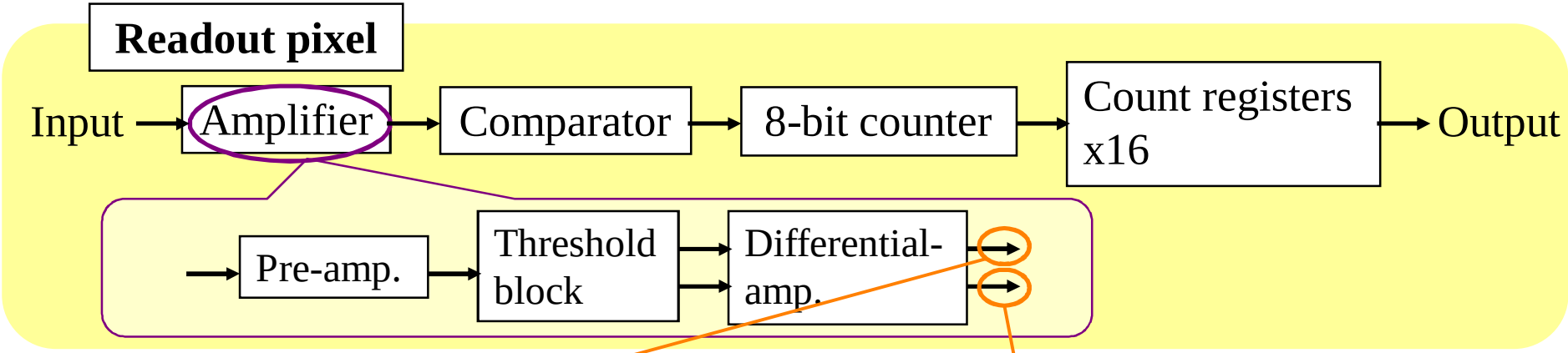


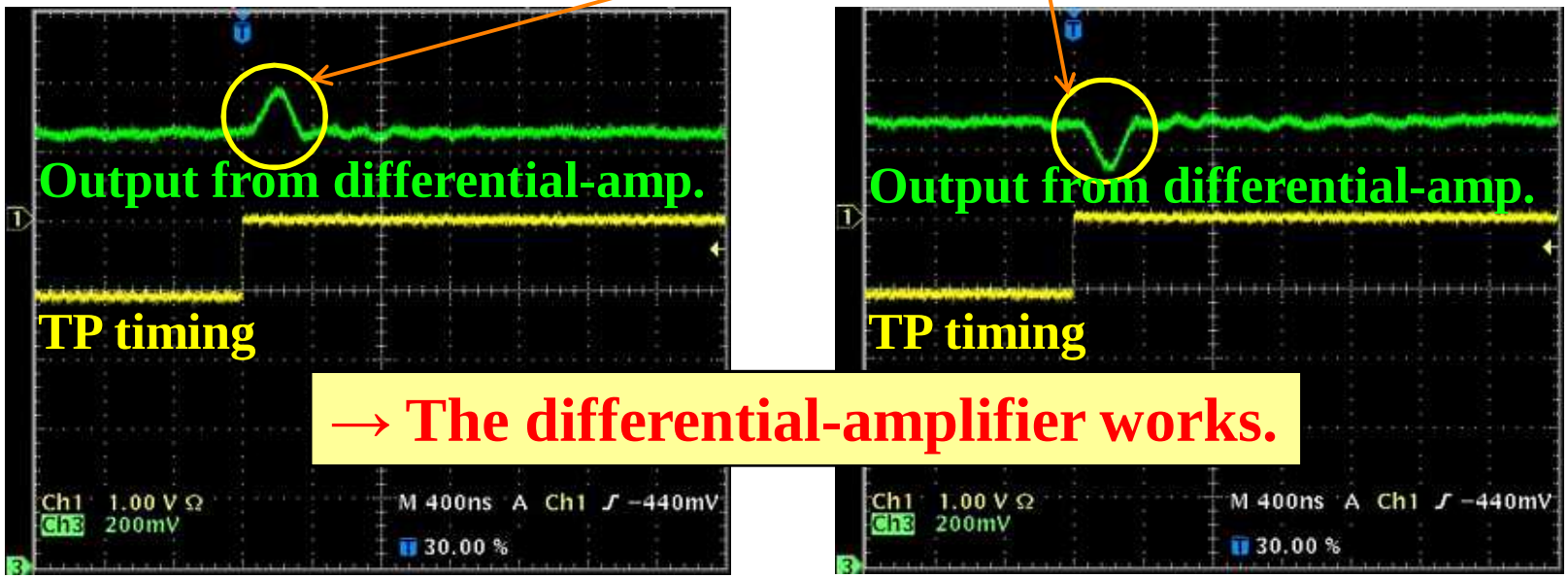
→ The pre-amplifier works.

Response of differential-amplifier

Operation test of the 3rd production

The response of the differential-amplifier was checked.

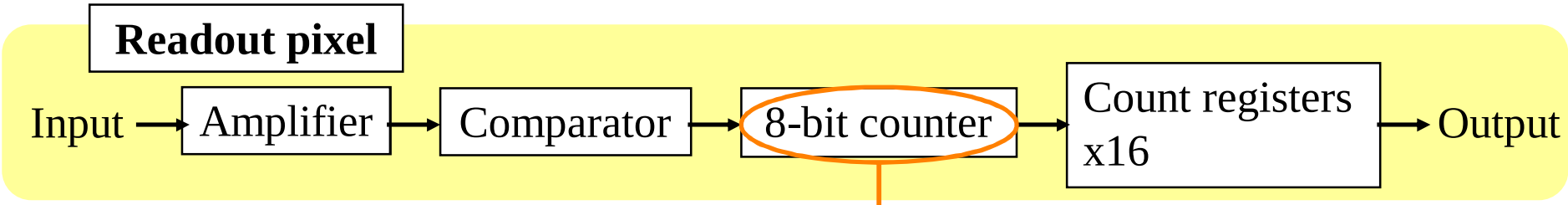




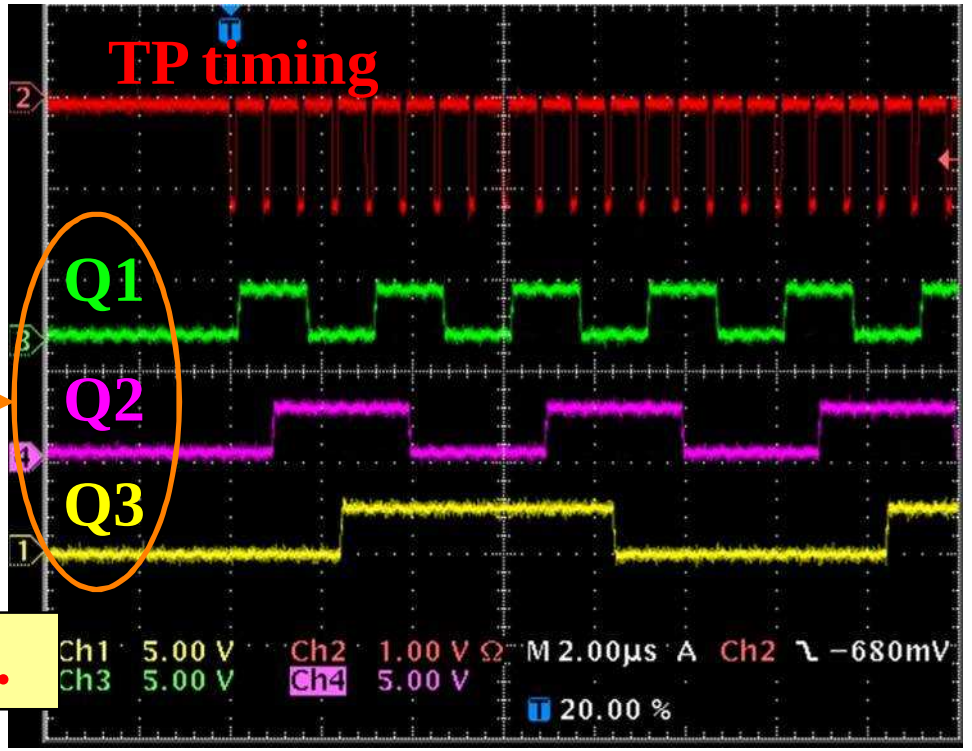
Response of counter block

Operation test of the 3rd production

The response of the counter was checked.



Gray code is used.



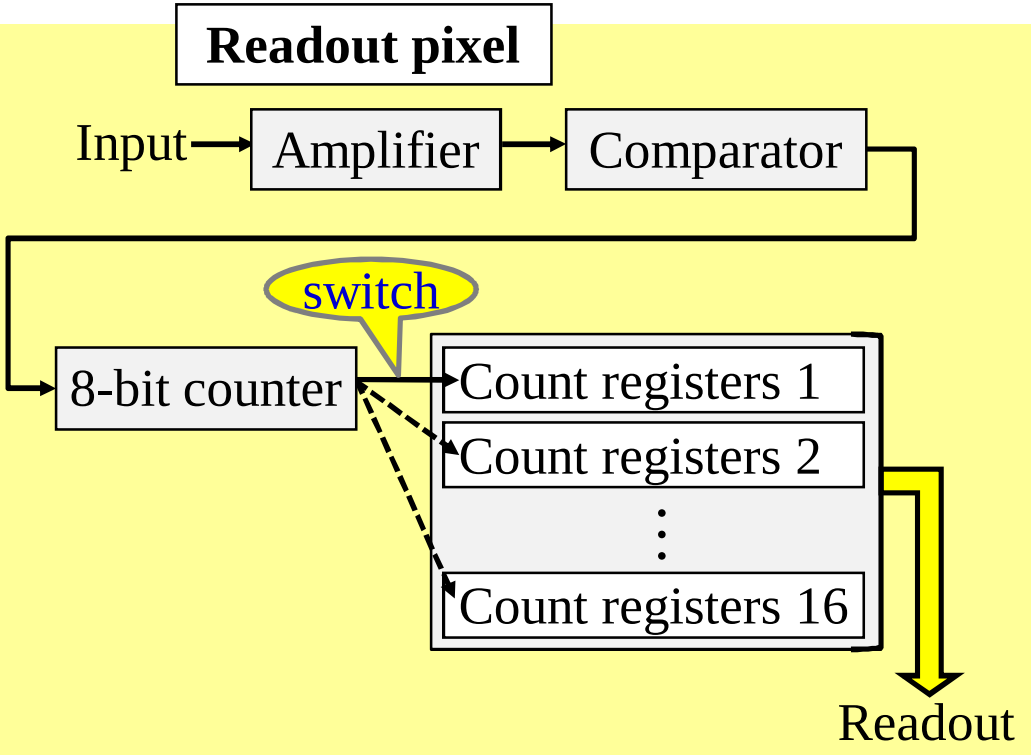
→ The counter works correctly.

Readout of hit counts

Operation test of the 3rd production

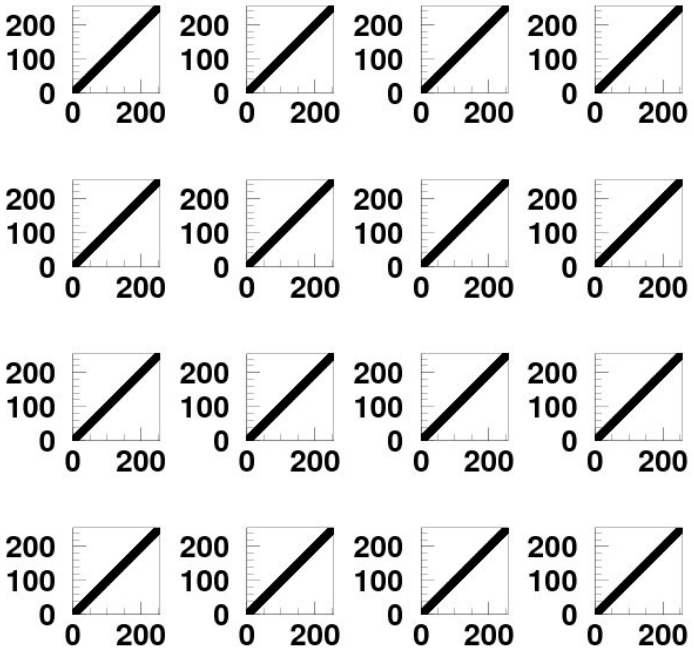
Readout of hit counts was checked.

- The hit count was stored at 2.5MHz hit rate/ (400μm x 400μm) and read out from the count registers.



# of input TP

v.s. # of readout hit counts



The readout ASIC was confirmed to work correctly as designed.

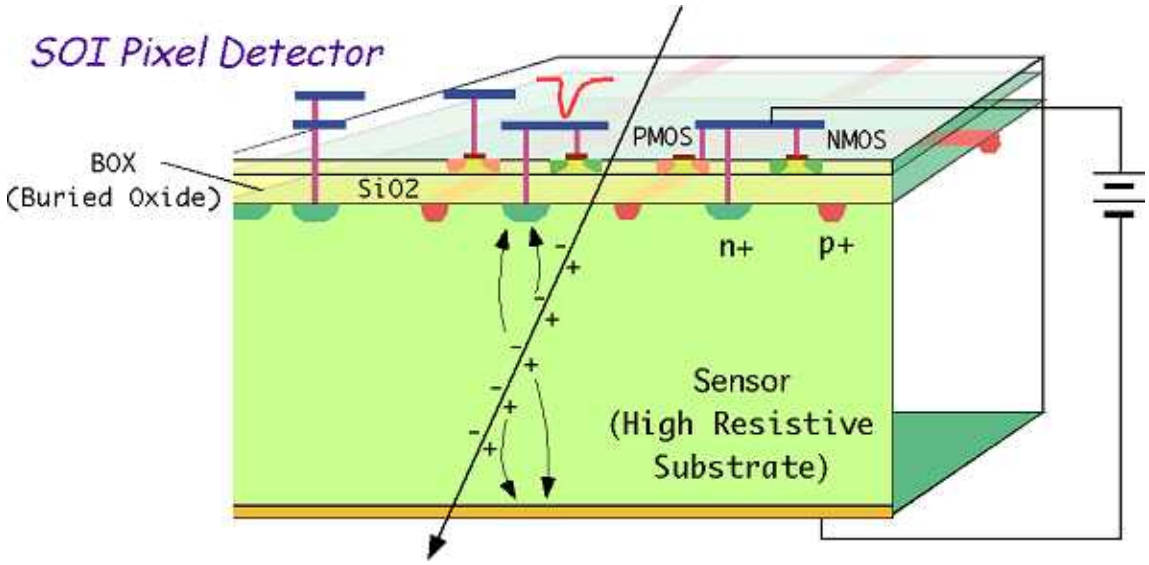
3. Pair-monitor with SOI technology

Pair-monitor with SOI technology

SOI (Silicon On Insulator) technology will be used
for the development of the pair-monitor.

SOI pixel detector

- The sensor and readout electronics are integrated
  in the SOI substrate. (monolithic)
  - High speed
  - Lower power
  - Thin device
  - Low material



The development of the Pair-monitor with SOI technology was started,
participating in MPW (Multi Project Wafer) Run at KEK.

Prototype of SOI chip

For the next prototype, only the readout ASCI will be developed.

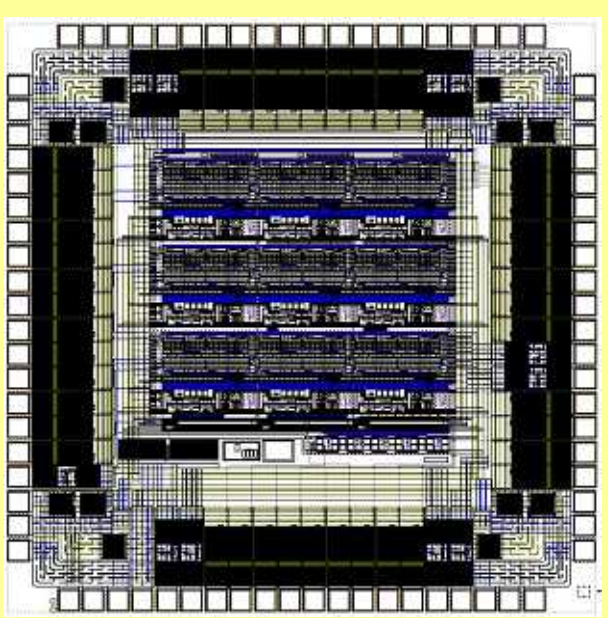
The layout of the readout ASIC was finalized.

Design of readout ASIC

- Production process : FD - SOI CMOS 0.2 μm
- Chip size : 2.5 x 2.5 mm^2
- # of pixel : 9 (= 3 x 3)

The chip will be delivered in Apr., 2009.

Layout of readout ASIC



4. Summary

Summary

- Beam profile monitor is necessary for high luminosity.

  → Pair-monitor
- The prototype of the readout ASIC was developed.
  - The chip works correctly as designed.
  - The chip will be connected with the PIN diode.
- The next readout ASIC will be developed

  with SOI technology.
  - The layout was finalized.
  - The prototype will be delivered in Apr., 2009.

Thank you for listening!