# Development of Readout system for FPCCD Vertex Detector

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## Outline

- FPCCD Vertex Detector
- Readout ASIC
- FPCCD readout test
- Summary

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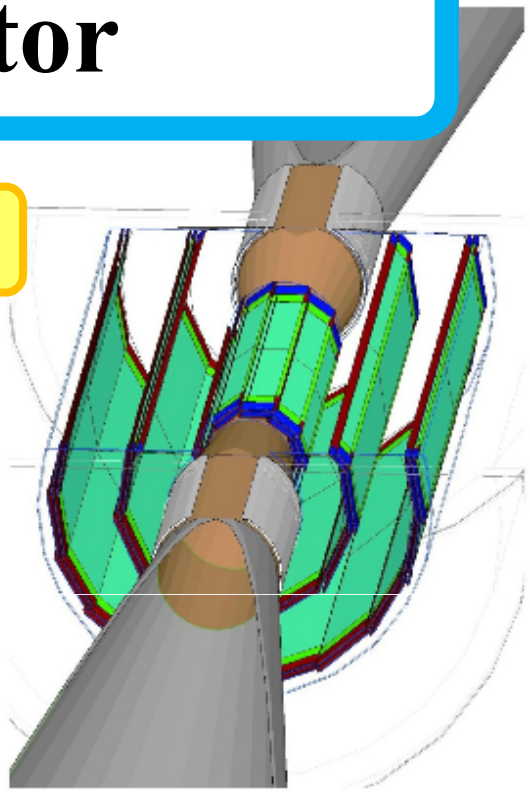
# FPCCD Vertex Detector

- FPCCD (Fine Pixel CCD)
  - ☛ Pixel size : **5μm × 5μm**
  - ☛ Sensitive thickness : 15 μm
- Total channel : 6080ch
  - ☛ 20000×128 pix/ch

  ⇒ Total pixel : ~$10^{10}$ pixel

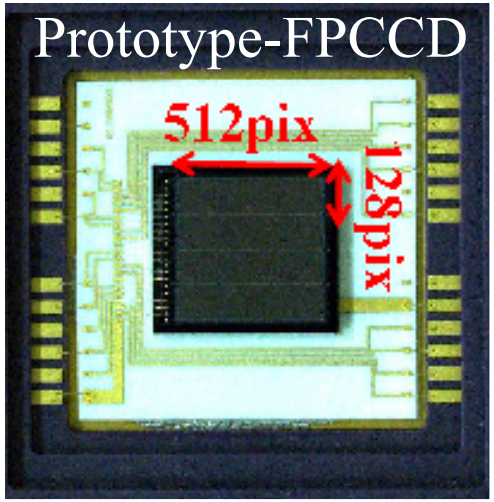
Full depleted

Very large



**Prototype-FPCCD to establish technology**

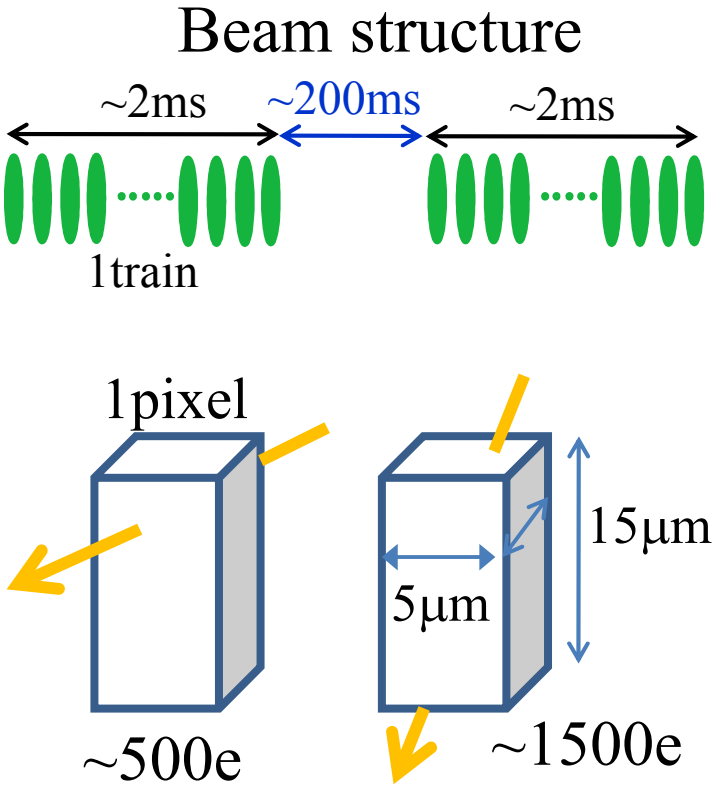
- ☛ Pixel size : **12μm × 12μm**
- ☛ Sensitive thickness : 15 μm
- ☛ Readout channel : 4ch
  - 512×128 pix/ch



# Requirements for FPCCD

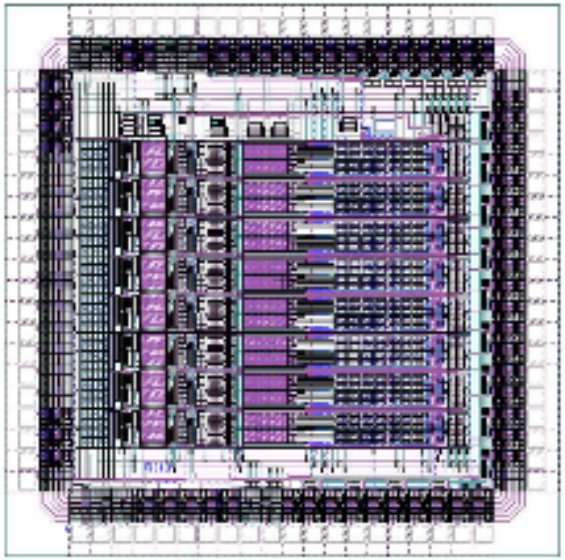
## Requirements for FPCCD

- Readout speed > 10Mpix/s
  - ☛ All pixels is read out in the inter-train time.
- Noise level < 50 electrons
  - ☛ Signal level is ~500e.
- Power Consumption < 100 W (16mW/ch)
  - ☛ VTX is put in cryostat.




**Readout ASIC was designed to satisfy these requirements.**

# Test of Readout ASIC

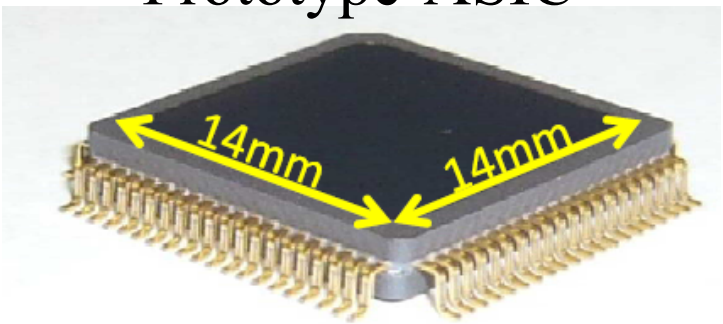


# Readout ASIC

## Requirements for ASIC

- Readout speed > 10 Mpix/sec
- Noise level < 30 electrons
- Power consumption < 6mW/ch

Prototype-ASIC

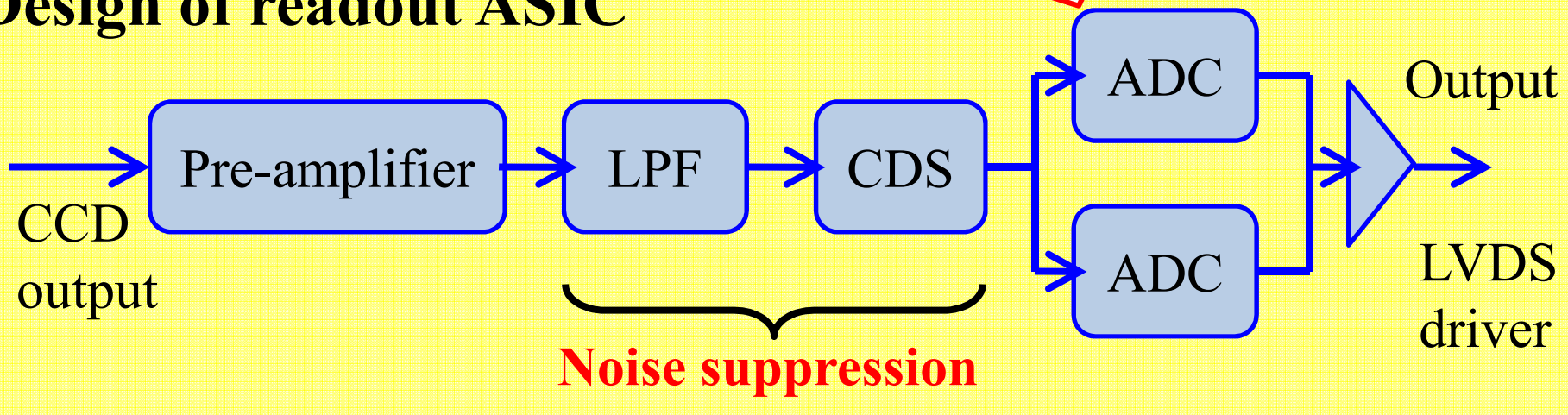



**Measures**

Charge sharing ADC
⇒ 10 μW/ch

5 Mpix/sec × 2

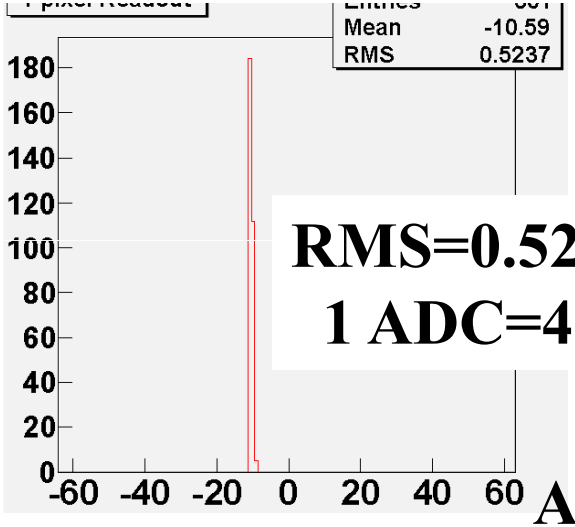
## Design of readout ASIC



# Performance of readout ASIC

Noise level of readout ASIC was measured.

**Pedestal distribution at 1.5Mpix/s**




**RMS=0.52**
**1 ADC=40e**

Noise level (Room temperature)
RMS = 0.52 ADC count
**~21 electrons** (Goal : 30 e)

The noise level satisfies the requirement.

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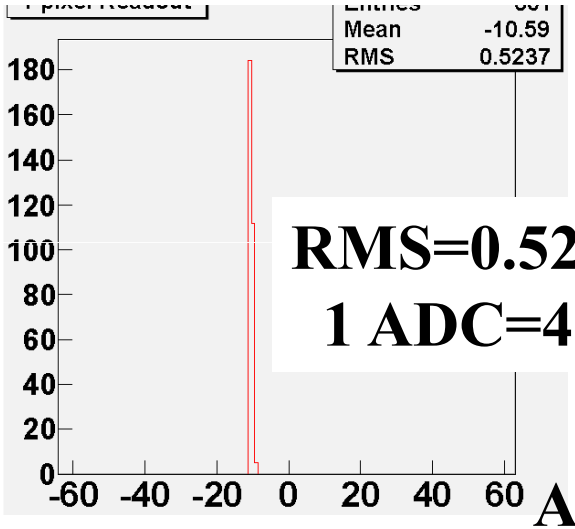


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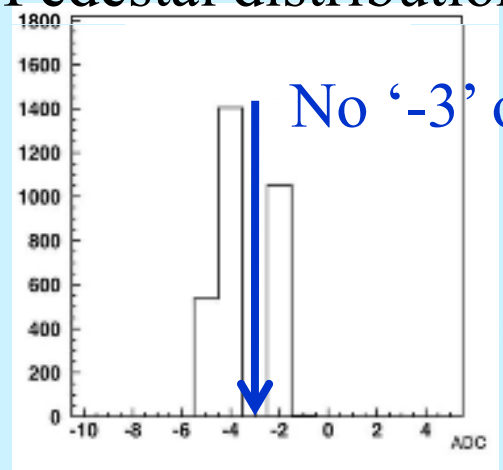
① Problem
Design value : 10Mpix/s

② Pedestal distribution




No '-3' output

Some ADC counts are missing.

The noise level satisfies the requirement.

# For next prototype-ASIC ①

The problems on the current ASIC will be solved in the **next ASIC**.

**Problem**

① **Readout speed : Max 1.5Mpix/s (Goal :10Mpix/s)**
② Some ADC counts don't output.

Solution to Problem①

The **current in the comparator** is **too small** for high speed readout.

**The power lines for ADC are increased**

Number of pad : 80 →100

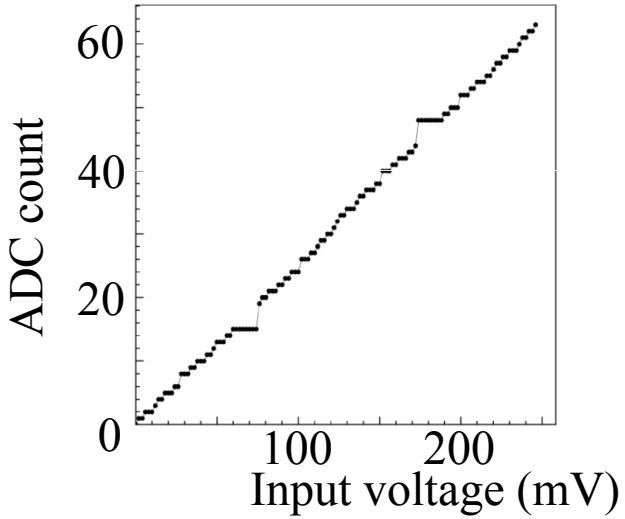
# For next prototype-ASIC ②

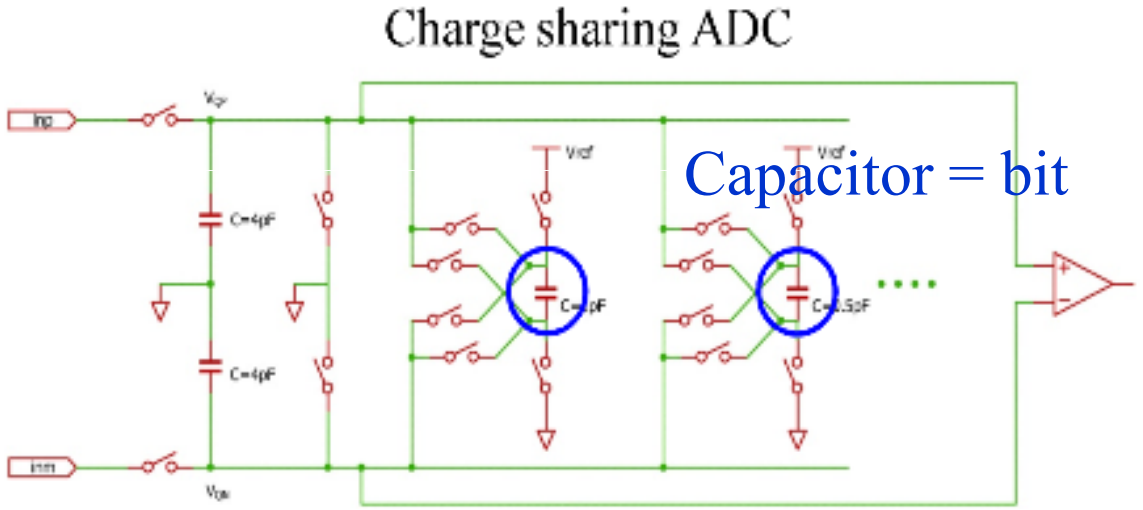
**Problem**

① Readout speed < 1.5Mpix/s (Goal :10Mpix/s)

② **Some ADC counts don't output.**

Solution to Problem②




The capacitance in ADC is shifted from design value by **the stray capacitance** in the switching circuits

⇨ **Number of transistors used in the switch ∝ Capacitance**

We will submit new ASIC modified on these problems on next February.

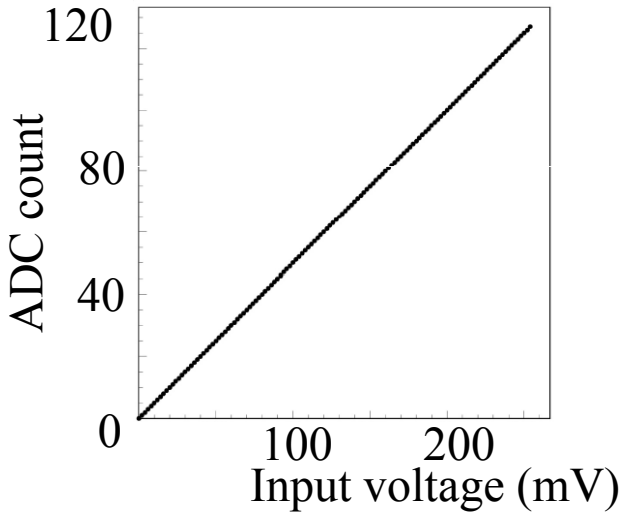
# For next prototype-ASIC ②

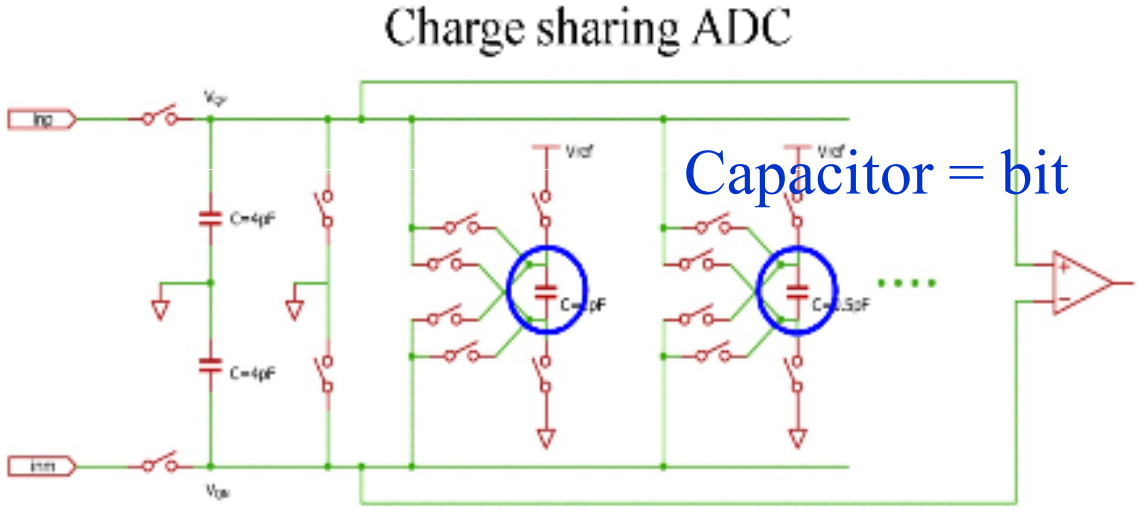
**Problem**

① Readout speed < 1.5Mpix/s (Goal :10Mpix/s)

② **Some ADC counts don't output.**

Solution to Problem②

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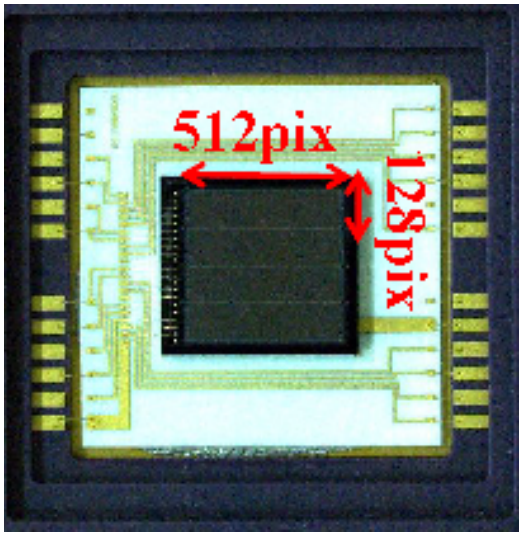
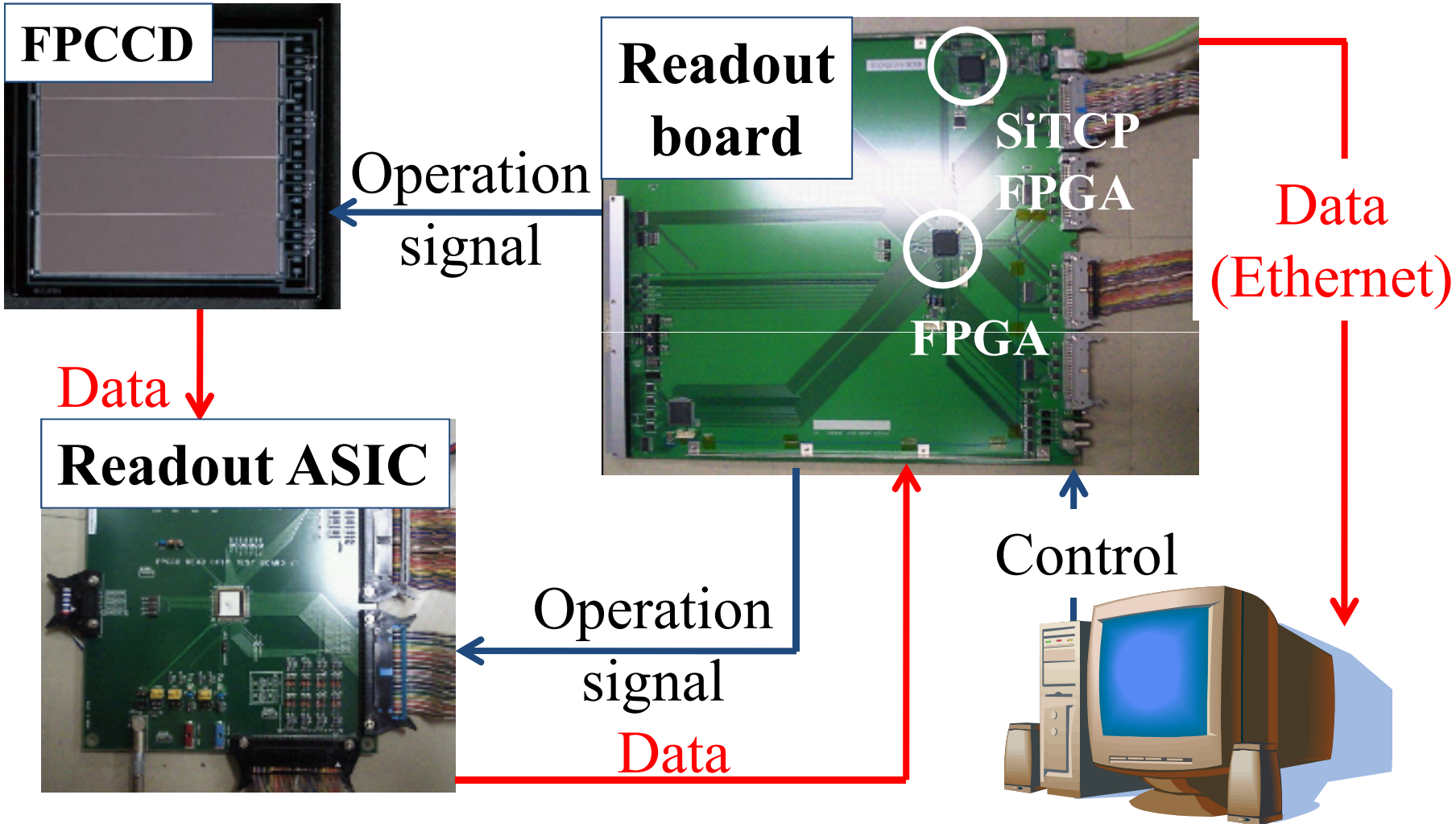
# Readout of FPCCD



# Test bench



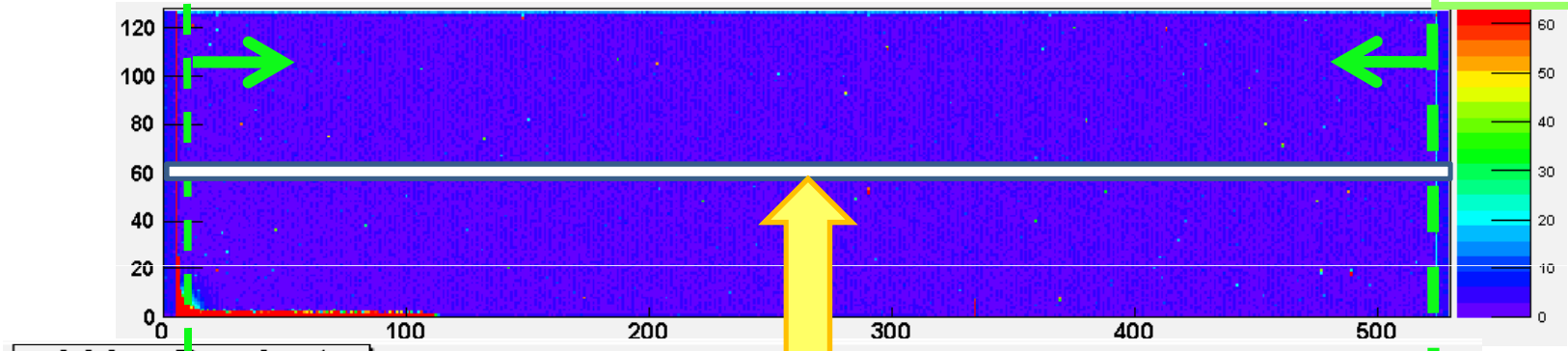

Readout test of FPCCD is performed by this test bench.

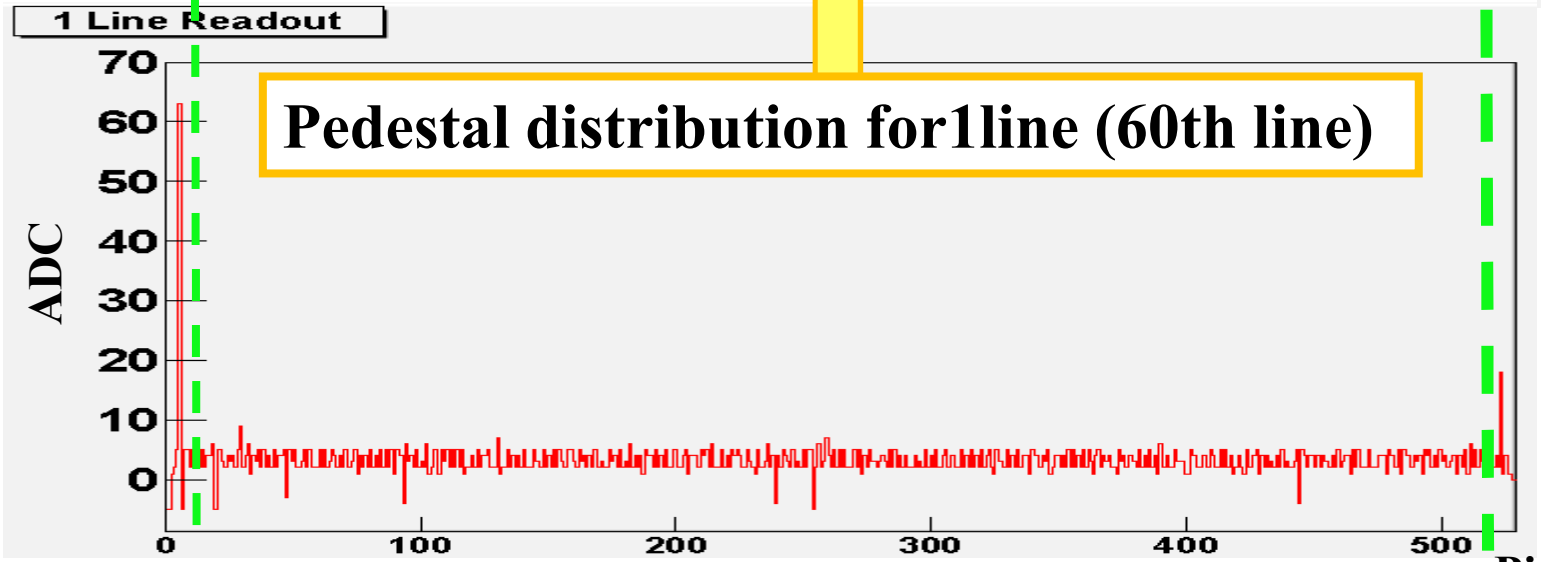
# CCD readout test : Pedestal

The pedestal of CCD is checked.

**CCD image of pedestal (ADC count)**

Sensor region



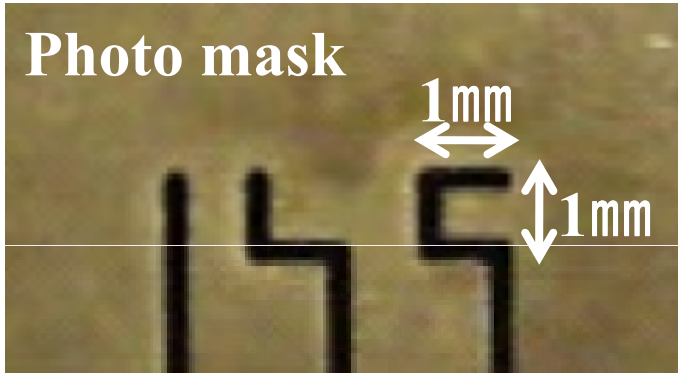




The difference between pixels is small.

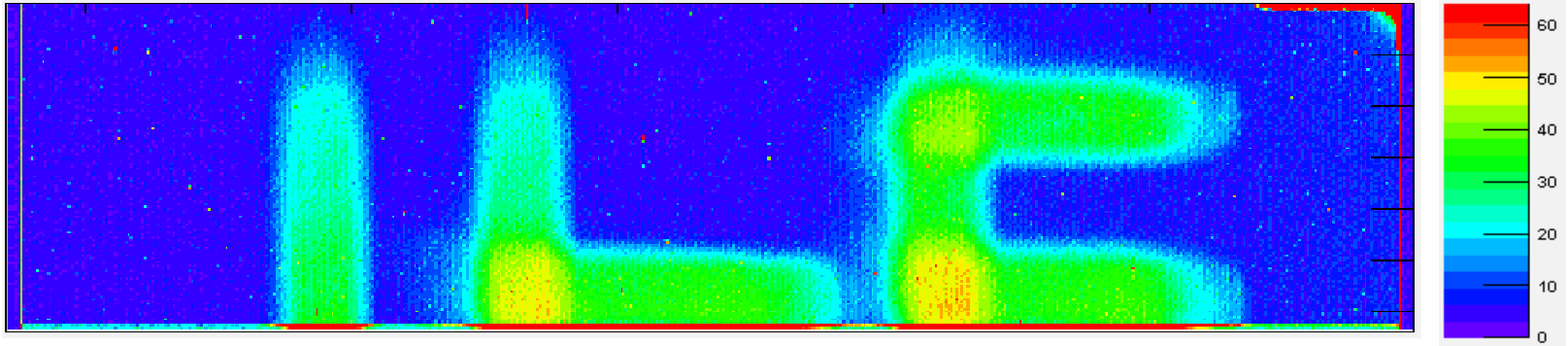
# CCD readout test : Test with LED

CCD is covered with the photo mask and radiated by LED light.

- Photo mask (made of brass)
  - ☞ Character size : 1mm×1mm
  - ☞ Line width : 0.2 mm




CCD image with photomask




**Success in reading “ILC” image ！**

# Summary and Plan

We have developed the readout system for FPCCD.

**Result of performance test**

- ☛ Readout ASIC
  - Readout speed : 1.5Mpix/sec (Goal : 10 Mpix/sec )
  - Noise level : 21eletrons (Goal : 30e)
- ☛ CCD sensor + Readout system
  - **Able to read picture**

**Plan**

- Readout ASIC

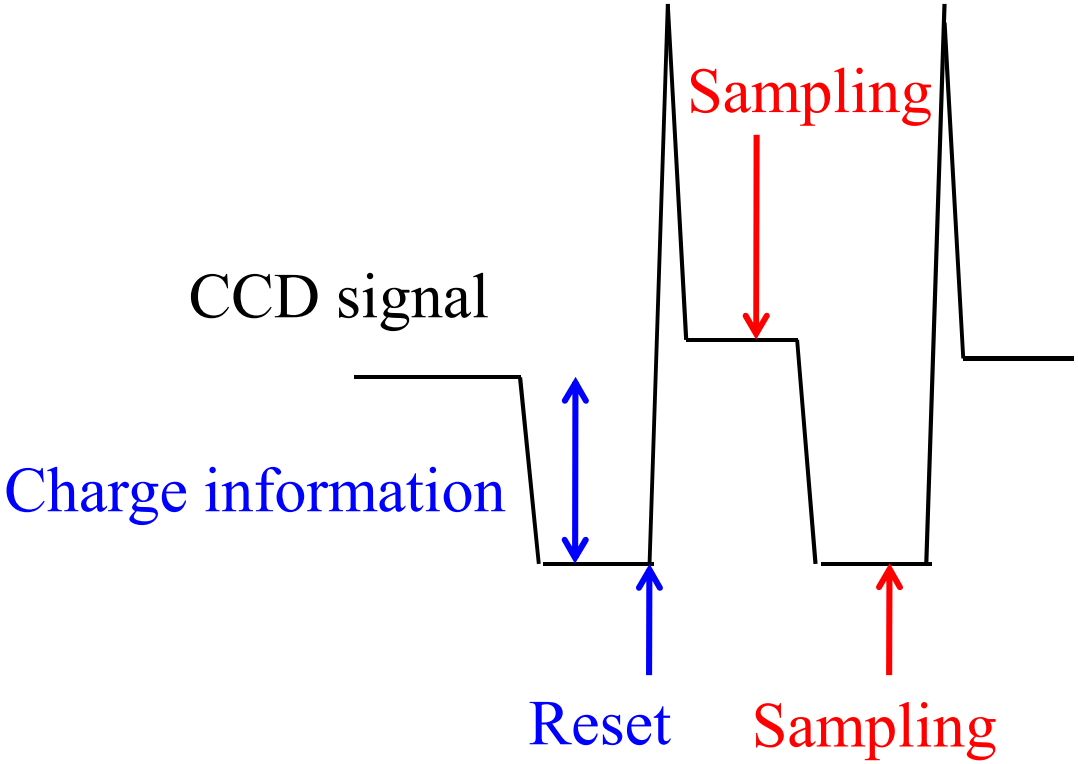
  Next prototype for ASIC will be made on next February

  ⇒Readout speed : **Our goal (10Mpix/sec) will be reached.**
- FPCCD readout test
  - Radiation test

# Back up

# Correlated double sampling circuit (CDS)

The difference on voltages between the reset and the signal level is measured.




Able to remove the noise from the amp and reset.

We can measure the only charge information of pixels.