

Do we need a pixel upgrade?

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A proposal for systematic simulation study for
vertexing upgrade.

+ A status report on pixel technology

♠: items needing MC study

Physics benefits of better vertex resolution
(apart from the obvious improvement in $\sigma_{\Delta z}$)

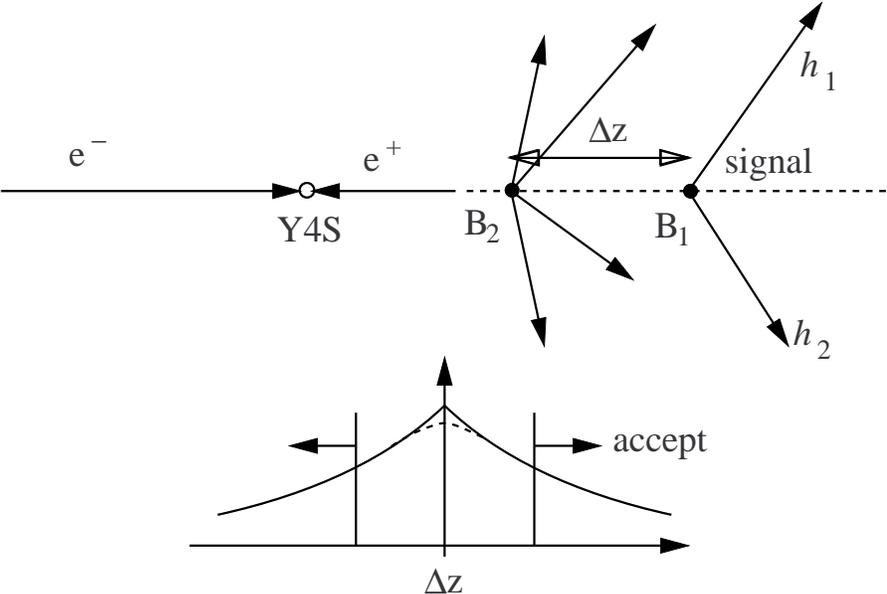
- Combinatorics
 - Inclusive (e.g. $K^{*0} \rightarrow K^- \pi^+$) ♠
 - $B \rightarrow D^0 D^-, D^+ D^-, D^0 K^-$ etc. ♠
- Charm vertex \rightarrow tag-side z resolution. ♠
- Vertical B travel: $\rightarrow \Delta z \rightarrow \Delta t$

Currently, the correction makes the resolution worse (crude calculation). ♠

- Continuum suppression by Δz ♠

Continuum suppression by z vertex separation

$$e^+e^- \rightarrow B_1B_2$$

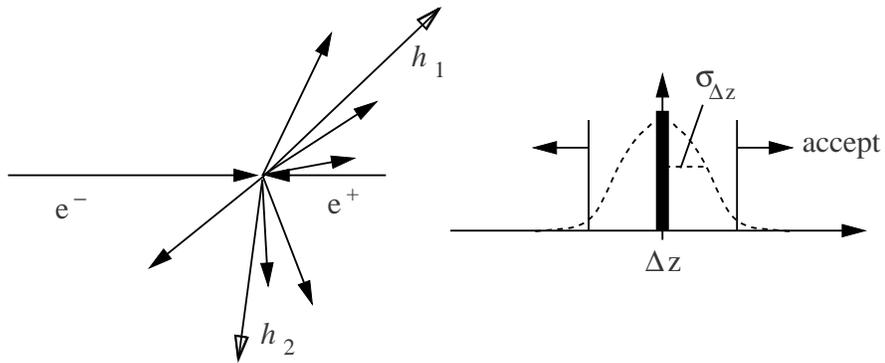


Δz distribution:

$$\propto \exp\left(-\frac{|\Delta z|}{L_0}\right)$$

$L_0(B \text{ mean decay length}) \sim 211\mu(Belle)$

$e^+e^- \rightarrow q\bar{q}$ (continuum)



Δz distribution (assume gaussian):

$$\propto \exp\left(-\frac{\Delta z^2}{2\sigma_{\Delta z}^2}\right)$$

$$\sigma_{\Delta z} \sim 125\mu$$

Discovery sensitivity improvement:

$\# \sigma$ probability of background fluctuate up to the signal.

$$\# \sigma = \frac{N_{\text{sig}}}{\sqrt{N_{\text{bkg}}}}$$

The improvement factor for $\# \sigma$ is then

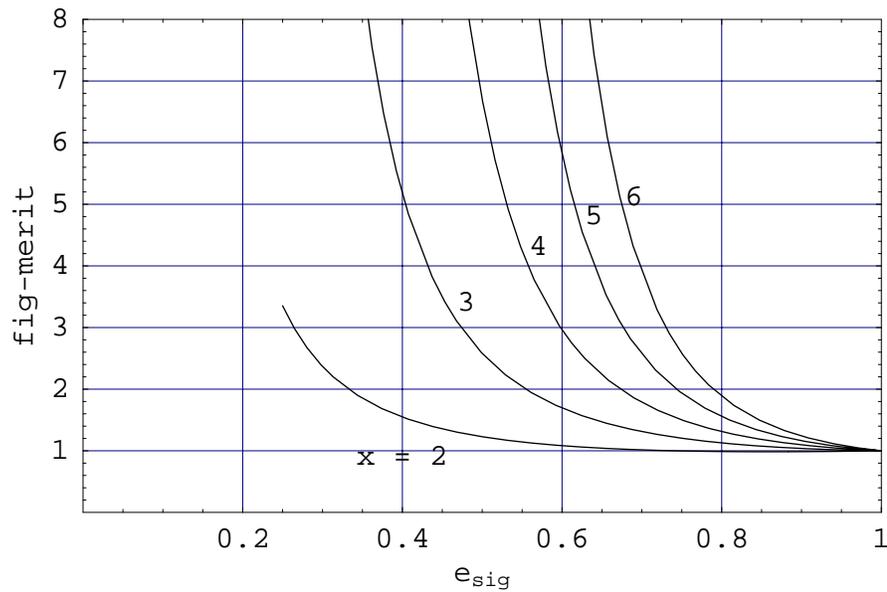
$$\text{fig. merit} = \frac{\epsilon_{\text{sig}}}{\sqrt{\epsilon_{\text{bkg}}}} \quad (\text{discovery})$$

Does not depend on $N_{\text{sig}}/N_{\text{bkg}}$ before the vertex separation cut.

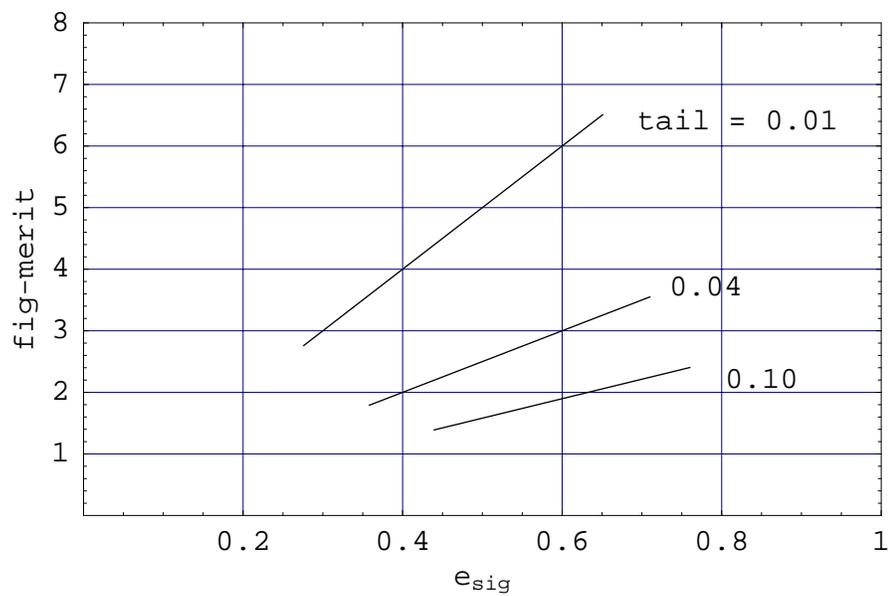
Discovery sensitivity improvement:

$$x \equiv \frac{L_0}{\sigma_{\Delta z}} \sim 2 \text{ for Belle, BaBar}$$

L_0 : B mean decay length (211 μ for Belle)



Tail: fraction of non-gaussian (\sim flat) tail of the Δz resolution.



Example: Can we find $B^- \rightarrow K^{*0}K^-$
if Br is 1/20 of $\rho^0\pi^-$? ♠

CLEO 2.5: $\rho^0\pi^-$ S/N $\sim 20/20$ @ 5 fb^{-1}

Assume factor of 4 reduction in bkg by a loose
particle ID cut.

$$\begin{aligned} &\rightarrow K^{*0}K^- \text{ S/N} \sim 1/5 \text{ @ } 5 \text{ fb}^{-1} \\ &\rightarrow K^{*0}K^- \text{ S/N} \sim 10/50 \text{ @ } 50 \text{ fb}^{-1} \end{aligned}$$

Significance = $10/\sqrt{50} = 1.4\sigma$: **Not a signal.**

With $\sigma_{\Delta z^-} > 1/2$ and 1% tail,

Significance $\rightarrow 1.4 \times 5.2 = 7.3\sigma$: **Clear signal.**

$K^{*0}K^-$ is an important mode to understand FSI,
annihilation diagram, and $b \rightarrow d$ penguin.

There are many important modes at this Br level:
 D^+K_S , D^0K^+ , $K^*\eta'$... Many of them play critical
roles in direct CP studies. ♠

Factor of 2 improvement in $\sigma\Delta z$ resolution can be achieved by (rough calculation)

- R_{beampipe} 2cm \rightarrow 1cm.
- 1/2 reduction of material (Si, support, beampipe).
- Keeping the same $\sigma_{\text{measurement}}$.

In general,

- σ_{measure} counts for high- P tracks ($P > 2$ GeV).
- Material reduction is important.
- R_{beampipe} reduction is essential.

Full MC study needed. ♠

Studies needed:

- Beam background control and IR design (incl. beampipe). 🚩
- Detector thin and tolerant of radiation/noise hits

Possible detector candidates for inner layers:
(e.g. 2 inner layers out of 5 total for vertexing)

1. Silicon strip
2. Pixel

Pros and cons of the pixel solution

Cons:

1. Requires substantial R& D to apply to Belle
(A few pixel detectors working in HEP experiments)
2. Readout electronics adds to the material budget
(could be as thin as a few 10's of μ ; will see)

Pros:

1. Measures true 3D points → noise hit tolerance

Assume 40 real hits on a $1 \times 3 \text{ cm}^2$ sensor.
(pitch: 50μ)

| occupancy | point hit | 3 pitches/hit |
|-----------|--------------------|--------------------|
| pixel: | 3×10^{-4} | 3×10^{-3} |
| strip: | 20% | 60% |

Needs realistic track finding simulation. ♠

2. Low capacitance per channel ($\ll 1 \text{ pF}$) → low noise

3. Low leakage current per channel ($\sim \text{fA}$) → low noise

Low noise partially translates to radiation tolerance.

A study on silicon strip detectors:

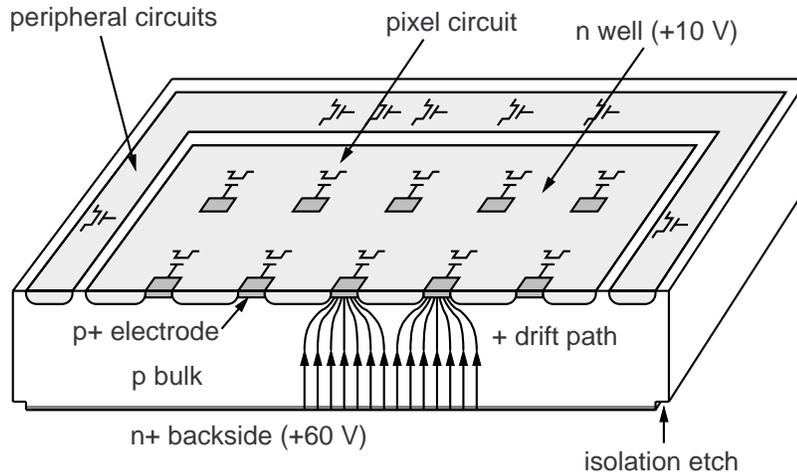
($1\text{cm} \times 1.3\text{cm}$, shaping time $0.7\mu\text{sec}$, ^{90}Sr)

| | | |
|-----|----------|----------|
| | 300μ | 100μ |
| S/N | 29.7 | 7.88 |

A large common-mode noise seen for 100μ sensor.

Monolithic Pixel Detector

Readout electronics and sensor on the same chip



Hawaii-Stanford monolithic pixel detectors
Fabricated at CIS, Stanford

- Thickness $300\mu\text{m}$
 - Collection electrode: p^+ (i.e. collects holes)
- Bulk: p
- Backside: n^+ -diffusion
- One PMOS readout circuit in n -well for each pixel.
- Operated with full depletion at $\sim 60\text{ V}$.

Two versions of monolithic pixel detector
successfully tested:

- V1.** 1993. Pitch $34 \times 125 \mu\text{m}^2$
1.02mm \times 1.02mm active area
Full readout
Tested at Fermilab (muon beam)
 $\rightarrow \sigma = 2.0 \mu\text{m}$ ($34 \mu\text{m}$ pitch direction)

- V2.** 1996. Pitch $65 \times 67 \mu\text{m}^2$
32 \times 32 array ($\sim 1\text{mm}^2$ active area)
Sparse readout
Tested by ^{241}Am

Challenges for the monolithic pixel design:

1. Larger array

Using the same sparse readout scheme, 320×320 array (1 cm^2), 0.5% pixel occupancy
→ $\sim 300 \mu\text{s}$ readout.

But, at this size most of the rows are hit (the sparse readout operates on rows) → might as well read all rows (future)

2. Foundry

Difficult to find a foundry who is

- willing to closely collaborate,
- has deep-submicron technology,
- can respond to non-standard fabrications:
rad-hard design, high-purity bulk silicon.

→ keep looking for a foundry,
but pursue hybrid design meanwhile.

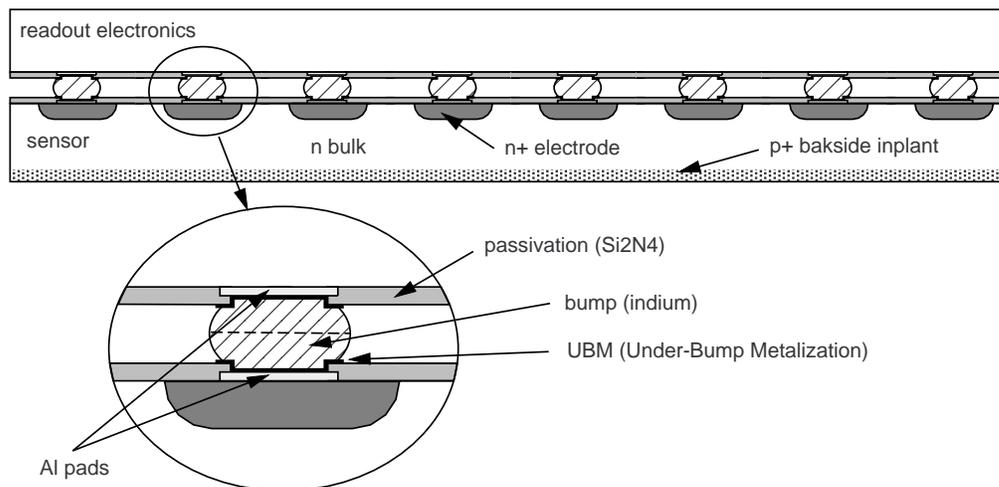
Hybrid Pixel Detectors

Hybrid = Bump-bonded

Sensor: high-resistivity silicon (typically float-zone)

Readout chip: Commercial CMOS OK

→ Fabricate separately and bond them
(flip-chip technology)



Most current and proposed HEP pixel detectors uses hybrid design.

(DELPHI, WA97, ATLAS, CMS., ALICE, BTeV...)

| | pixel size | # pixel (total) | sensor thickness | heat/cell |
|--------|--|--------------------|----------------------|-------------------|
| DELPHI | $330 \times 330 \mu^2$ | 1.2 M | 300μ | $40 \mu\text{W}$ |
| WA97 | $50 \times 500 \mu^2$ $75 \times 500 \mu^2$ | 1.2 M | 300μ | |
| ATLAS | $50 \times 300 \mu^2$ | 105 M | $200\text{-}250 \mu$ | $50 \mu\text{W}$ |
| CMS | $150 \times 150 \mu^2$ | 56 M | $200\text{-}250 \mu$ | $60 \mu\text{W}$ |
| ALICE | $50 \times 300 \mu^2$ | 15.7 M | 150μ | $30 \mu\text{W}$ |
| BTeV | $50 \times 300 \mu^2$ | 60 M | 300μ | $<40 \mu\text{W}$ |

Issues for a Belle pixel detector:

- (a) Readout electronics (that fits in $50 \times 50 \mu^2$)
- (b) Thinning of sensor and readout chips
- (c) Bump bonding
- (d) Radiation hardening

(a) Proposed readout electronics
(Conceptual design by G. Varner)

- Avoid sending analog signal by digitizing on each pixel.
- V_{ramp} + Comparator and 5-line counting bus.
LVDS driver at the end of sensor.
- $1\text{cm} \times 3\text{cm}$, $50 \times 50 \mu\text{m}^2$ pixel.
2% occupancy \rightarrow $200 \mu\text{s}$ read out time.

Expected heat generation

- Most of the time the MOS transistors do not dissipate heat, namely static.
(much easier situation than LHC)
- Needs a completed design of the circuit,
but roughly, $\sim 0.4\mu\text{W}/\text{pixel}$
 $\rightarrow \Delta T \sim 0.1^\circ\text{K}$ (side cooling)
- LVDS driver generates lots of heat, but it is at the end of sensor.

(b) Thinning of the sensor and readout chip

- Wafer thinning is a routine commercial process (for heat dissipation)

{ Grinding-polishing-etching
{ Plasma etching

- Readout electronics:
Thinned after fabrication using a commercial process (e.g. MOSIS).
- Sensors may be thinned first.
(needs a dedicated foundry)
Or, thinned after fabrication
(still needs some processing of the thinned side)
- Thin before or after the bump bonding?
If thinned after bonding, the read-out electronics may be made quite thin ($\sim 20\mu?$).
→ **more R& D needed.**

(c) Bump bonding

- Bump bonding defects $< 10^{-4}$ (dummy tests).
But some problems reported for the real ATLAS detector.
- Bump diameter can be $< 10\mu$,
pitch can be $< 20\mu$
(e.g. GEC Marconi)

Two types of bumps

| | Indium | Solder |
|---|------------------------|---------------------------------|
| UBM * | simple | complicated |
| bump deposition | both sides | one side |
| connection | pressure | fused |
| Strength (4K bumps) (tension& shear) | 2.5 lb | 10-14 lb (strong) |
| alignment required | 1-2 μ | $\sim 10\mu$ (self-aligning) |
| resistance/bump | 1-2 Ω (poor) | 2-3 $\mu\Omega$ (good) |

* UBM = Under Bump Metalization

(d) Radiation Hardening

Radition damage effects

- a) Effective dopant creation
- b) Leakage current increase
- c) Threshold shift of MOS transistors

a) Effective dopant creation

Mostly p type

- Change in $V_{\text{depletion}}$ (e.g. increase)
→ high voltage breakdown, partial depletion
- Type conversion ($n \rightarrow p$) at high dose
(OK for Belle)

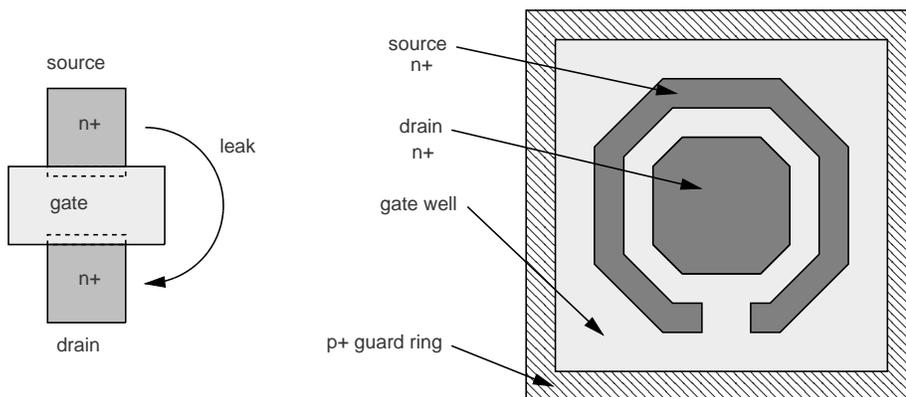
→ Design the detector such that it can stand high voltage
(e.g. guard rings at the edges of sensor)

b) Leakage current

1. source-drain leakage
2. inter-transistor leakage
3. detector bulk leakage current

Strategy:

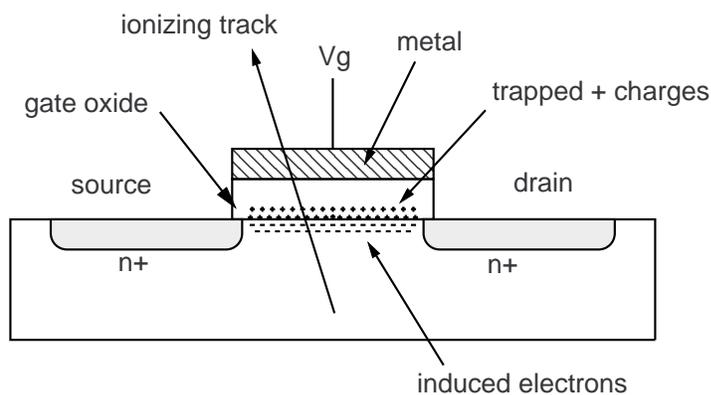
- Rad-hard design rules
 - * Surround-gate design
 - * *p*-stop around NMOS transistor



- current compensation for detector leakage (read-out electronics design)

c) Threshold shift of MOS transistor

Trapped positive ionization charges at gate-oxide
→ induces electrons just below the gate.



$$\Delta V_{th} \propto \begin{cases} t^2 & (t < 10 \text{ nm}) \\ t^3 & (t < 10 \text{ nm}) \end{cases}$$

t : gate thickness

Make the gate oxide thin:

← natural result of small scale processes.

(e.g. commercial IBM 0.25 μ process)

Pixel detector status summary:

1. Monolithic pixel proven to work (32×32 array).

- larger detector
- Challenges: ● rad-hardness
- **foundry !!**

→ try hybrid design.

2. Hybrid pixel design

- heat $< 50\mu\text{W}/\text{pixel}$ for LHC.
Less for Belle → probably not a problem.
- thickness $< 250\mu$ (sensor & read-out)
being tested. 150μ total seems feasible.
- bump bonding
yield $> 99.99\%$:dummy test
(some problems with real detectors)
pad size can be $< 10\mu$, pitch can be $< 20\mu$
- Rad-hardness of readout chip
Deep sub μ + rad.hard rules →
30 MRad : IBM 0.25μ (ALICE)
(Barely fits in $50 \times 300\mu^2$)

R& D Items Summary:

1. Readout electronics that fits in pixel and rad-hard.
2. Thinning of sensor ($\sim 100\mu$) and readout chip ($\sim 50\mu$).
3. Bump bonding for our specifics.

On-going efforts:

Prototype design

2mm \times 2mm

pixel: $50\mu \times 100\mu$

- Readout electronics design by G. Varner. MOSIS submission in a few months.
- Sensor design by S. Parker and C. Kenney. To be fabricated at CIS in the same time scale.
- Bump-bonding test: in contact with GEC Marconi. Other companies are to be tested.