Improved Vertexing for Belle (and also for NLC)

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Two Fronts

(A) Strip detector upgrade

Radhardization of readout chip

Process: 1.2μm → 0.8μm
VA1(1.2μ) (old) limit $\sim$ 200 KRad
VA1(0.8μ) (new) limit $\sim$ 1 MRad

VA1(0.8μ) will be installed as SVD1.5 in 2000.

VA1(0.6μ) under study (SVD 2.0?)

(B) Pixel detector R&D

Physics benefits of better vertex resolution (apart from the obvious improvement in $\sigma_{\Delta z}$)

- Combinatorics
  - ○ Inclusive (e.g. $K^{*0} \to K^-\pi^+$) ♠
  - ○ $B \to D^0 D^-, D^+ D^-, D^0 K^-$ etc. ♠

- Charm vertex → tag-side z resolution. ♠

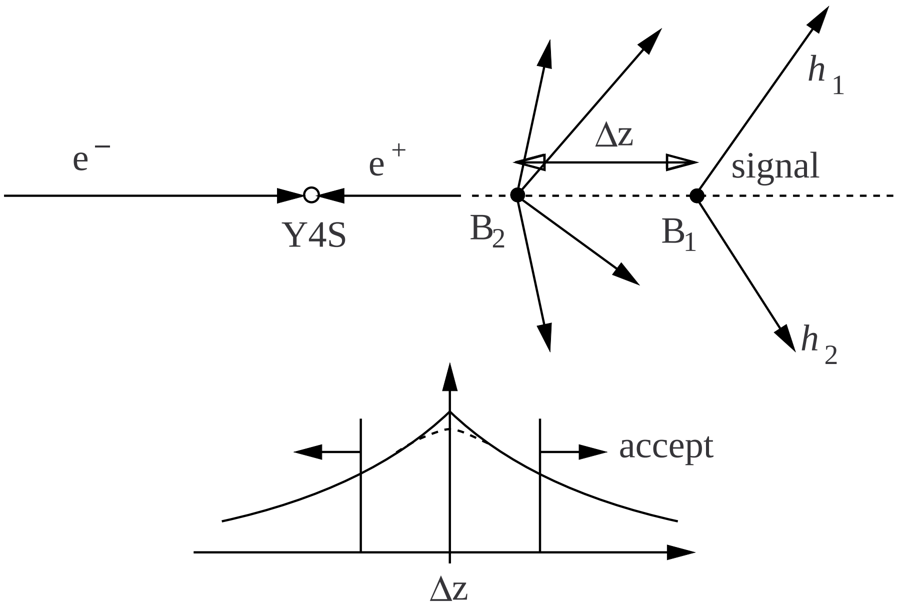
- Vertical B travel: $\to \Delta z \to \Delta t$

  Currently, the correction makes the resolution worse (crude calculation). ♠

- Continuum suppression by Δz ♠

Continuum suppression by z vertex separation

$$e^+e^- \to B_1B_2$$

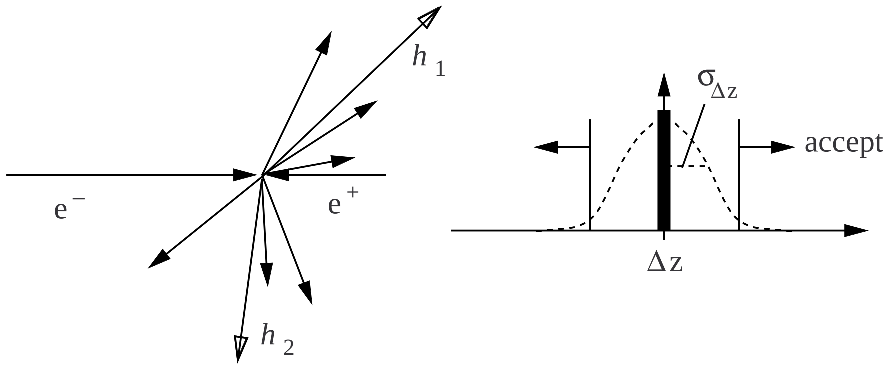


Δz distribution:

$$\propto \exp\left(-\frac{|\Delta z|}{L_0}\right)$$

L_O(B mean decay length) $\sim 211\mu(Belle)$

$e^+e^- \to q\bar{q}$ (continuum)



Δz distribution (assume gaussian):

$$\propto \exp\left(-\frac{\Delta z^2}{2\sigma_{\Delta z}^2}\right)$$

$$\sigma_{\Delta z} \sim 125\mu$$

Discovery sensitivity improvement:

$\#\sigma$ probability of background fluctuate up to the signal.

$$\#\sigma = \frac{N_{\text{sig}}}{\sqrt{N_{\text{bkg}}}}$$

The improvement factor for $\#\sigma$ is then

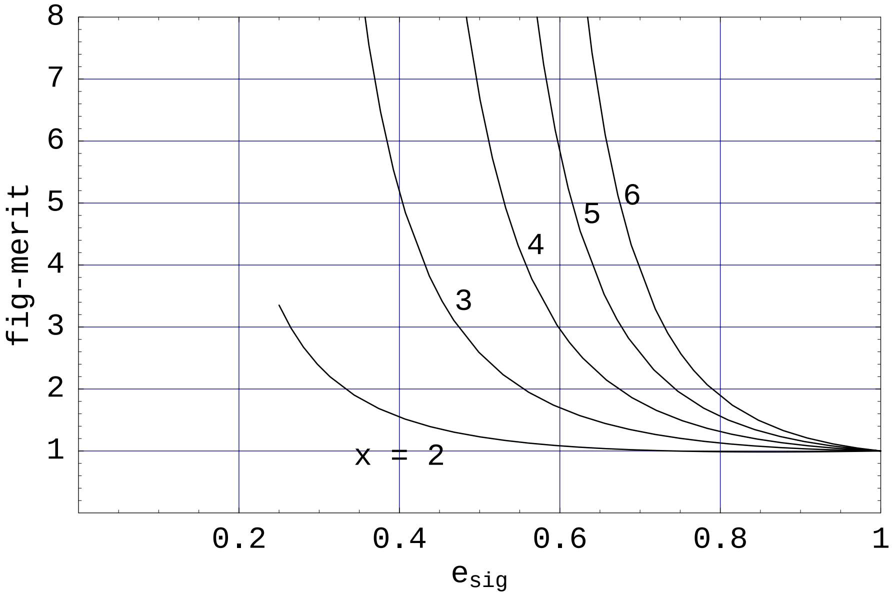
$$\boxed{\text{fig. merit} = \frac{\epsilon_{\text{sig}}}{\sqrt{\epsilon_{\text{bkg}}}}} \quad \text{(discovery)}$$

Does not depend on $N_{\text{sig}}/N_{\text{bkg}}$ before the vertex separation cut.

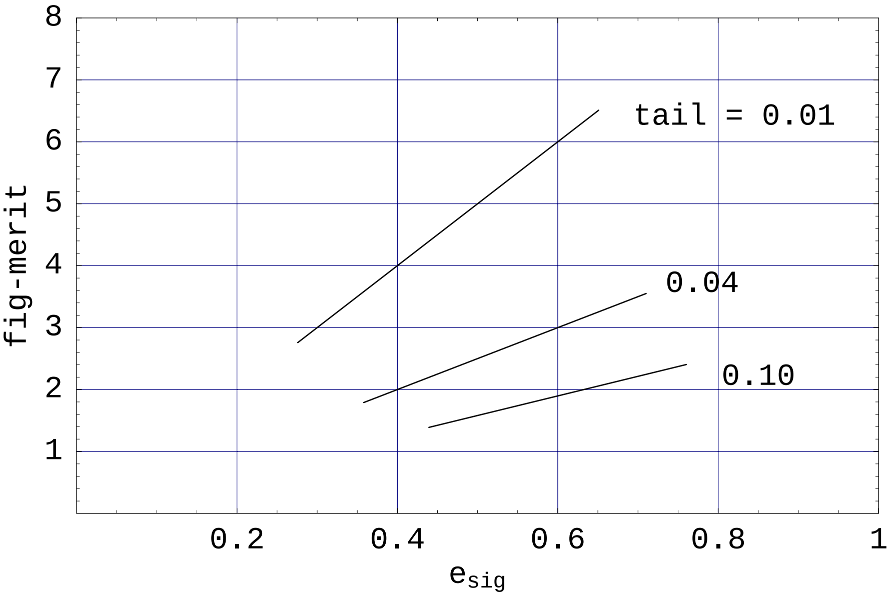
Discovery sensitivity improvement:

$$x \equiv \frac{L_0}{\sigma_{\Delta z}} \quad \sim 2 \text{ for Belle, BaBar}$$

L_0: B mean decay length (211 μ for Belle)



Tail: fraction of non-gaussian ($\sim$ flat) tail of the Δz resolution.



Example: Can we find $B^- \to K^{*0}K^-$ if Br is 1/20 of $\rho^0\pi^-$? ♠

CLEO 2.5: $\rho^0\pi^-$ S/N $\sim$ 20/20 @ 5 fb^{-1}

Assume factor of 4 reduction in bkg by a loose particle ID cut.

$\to K^{*0}K^-$ S/N $\sim$ 1/5 @ 5 fb^{-1}
$\to K^{*0}K^-$ S/N $\sim$ 10/50 @ 50 fb^{-1}

Significance $= 10/\sqrt{50} = 1.4\sigma$: Not a signal.

With $\sigma_{\Delta z} -> 1/2$ and 1% tail,

Significance $\to 1.4 \times 5.2 = 7.3\sigma$: Clear signal.

$K^{*0}K^-$ is an important mode to understand FSI, annihilation diagram, and $b \to d$ penguin.

There are many important modes at this Br level: D^+K_S, D^0K^+, $K^*\eta'$ ... Many of them play critical roles in direct CP studies. ♠

Factor of 2 improvement in $\sigma\Delta z$ resolution can be achieved by (rough calculation)

- R_{beampipe} 2cm → 1cm.
- 1/2 reduction of material (Si, support, beampipe).
- Keeping the same $\sigma_{\text{measurement}}$.

In general,

- σ_{measure} counts for high-P tracks ($P > 2$ GeV).
- Material reduction is important.
- R_{beampipe} reduction is essential.

Full MC study needed. ♠

Studies needed:

- Beam background control and IR design (incl. beampipe). ♠
- Detector thin and tolerant of radiation/noise hits

Possible detector candidates for inner layers:
(e.g. 2 inner layers out of 5 total for vertexing)

1. Silicon strip
2. Pixel

Pros and cons of the pixel solution

Cons:

1. Requires substantial R& D to apply to Belle
   (A few pixel detectors working in HEP experiments)

2. Readout electronics adds to the material budget
   if hybrid design.
   (readout chip could be as thin as
   a few 10's of μ; will see)

Pros:

1. Measures true 3D points → noise hit tolerance

   Assume 40 real hits on a 1×3 cm^2 sensor.
   (pitch: 50μ)

occupancy	point hit	3 pitches/hit
pixel:	3×10^{-4}	3×10^{-3}
strip:	20%	60%

   Needs realistic track finding simulation. ♠

2. Low capacitance per channel ($\ll 1$ pF) → low noise

3. Low leakage current per channel ($\sim$ fA) → low noise

   Low noise partially translates to radiation tolerance.

A study on a thin silicon strip detectors:
(1cm$\times$1.3cm, shaping time 0.7μsec, ^{90}Sr)

	300μ	100μ
S/N	29.7	7.88

A large common-mode noise seen for 100μ sensor.

→ We Need a Pixel Detector for Belle

Essential point:

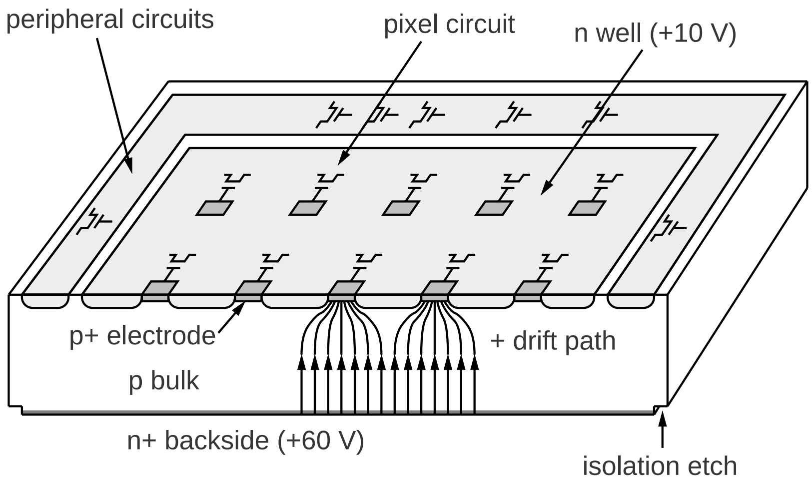
- We need a substantial improvement in vertex resolution
  - to make the best use of B-factory
  - to compete

- A pixel detector will make it possible by allowing us to get closer to the beam.

Plan: Install as the inner few layers of a future vertexing system.

Monolithic Pixel Detector

Readout electronics and sensor on the same chip



Hawaii-Stanford monolithic pixel detectors
Fabricated at CIS, Stanford

- Thickness 300μm
- Collection electrode: p^+ (i.e. collects holes)
  Bulk: p
  Backside: n^+-diffusion
- One PMOS readout circuit in n-well for each pixel.
- Operated with full depletion at $\sim$60 V.

Two versions of monolithic pixel detector succesfully tested:

V1. 1993. Pitch $34 \times 125\mu\text{m}^2$
1.02mm×1.02mm active area
Full readout

Tested at Fermilab (muon beam)
$\rightarrow \sigma = 2.0\mu\text{m}$ ($34\mu\text{m}$ pitch direction)

V2. 1996. Pitch $65 \times 67\mu\text{m}^2$
32×32 array ($\sim 1\text{mm}^2$ active area)
Sparse readout
Tested by ^{241}Am

Challenges for the monolithic pixel design:

1. Larger array

Using the same sparse readout scheme, 320×320 array (1 cm^2), 0.5% pixel occupancy
→ ∼ 300μs readout.

Full readout?

2. Foundry

Difficult to find a foundry who is

- willing to closely collaborate,
- has deep-submicron technology,
- can respond to non-standard facbrications: rad-hard design, high-purity bulk silicon.

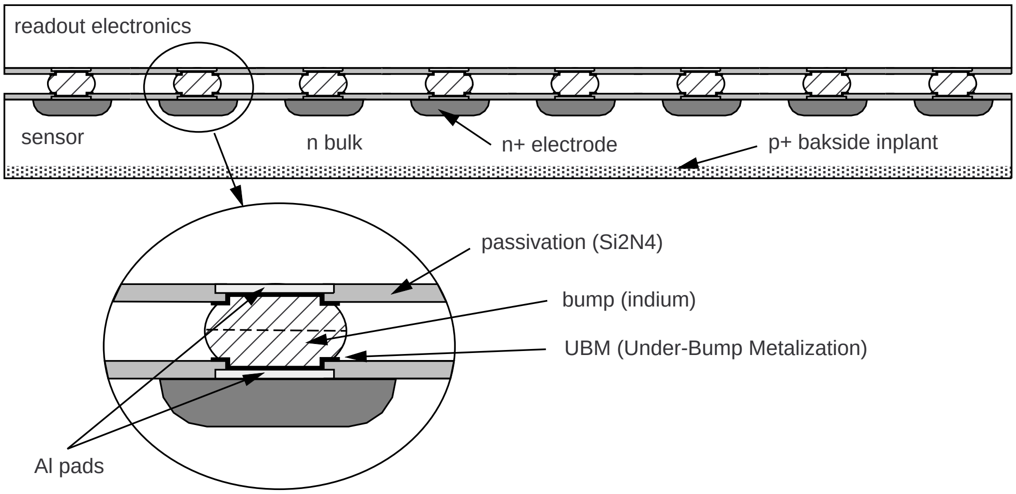
→ keep looking for a foundry...

Hybrid Pixel Detectors

Hybrid = Bump-bonded

Sensor:high-resistivity silicon (typically float-zone)
Readout chip: Commercial CMOS OK

→ Fabricate separately and bond them
(flip-chip technology)



Most current and proposed HEP pixel detectors uses hybrid design.
(DELPHI, WA97, ATLAS, CMS., ALICE, BTeV...)

	pixel size	# pixel (total)	sensor thickness	heat/cell
DELPHI	$330\times330\mu^2$	1.2 M	300μ	40μW
WA97	$50\times500\mu^2$ $75\times500\mu^2$	1.2 M	300μ	
ATLAS	$50\times300\mu^2$	105 M	200-250μ	50μW
CMS	$150\times150\mu^2$	56 M	200-250μ	60μW
ALICE	$50\times300\mu^2$	15.7 M	150μ	30μW
BTeV	$50\times300\mu^2$	60 M	300μ	$<40\mu$W

Issues for a Belle pixel detector:

(a) Readout electronics (that fits in $\sim 40 \times 60\mu^2$)

(b) Thinning of sensor and readout chips

(c) Bump bonding

(d) Radiation hardening

(a) Proposed readout electronics

(by G. Varner)

- Avoid sending analog signal by digitizing on each pixel.
- V_{ramp}+Comparator and 5-line counting bus.
  LVDS driver at the end of sensor.
- 1cm×3cm, start from $50 \times 100\mu\mathrm{m}^2$ pixel.

Expected heat generation

- Most of the time the MOS transistors do not dissipate heat, namely static.
  (much easier situation than LHC)

- $\sim$0.4μW/pixel
  $\rightarrow \Delta T \sim$ 0.1°K (side cooing)

- LVDS driver generates lots of heat, but it is at the end of sensor.

(b) Thinning of the sensor and readout chip

- Wafer thinning is a routine commercial process (for heat dissipation)

$$\begin{cases}\text{Grinding-polishing-etching}\\ \text{Plasma etching}\end{cases}$$

- Readout electronics:

  Thinned after fabrication using a commercial process (e.g. MOSIS).

- Sensors may be thinned first.
  (needs a dedicated foundry)

  Or, thinned after fabrication
  (still needs some processing of the thinned side)

- Thin before or after the bump bonding?

  If thinned after bonding, the read-out electronics may be made quite thin ($\sim 20\mu$?).

  → **more R&D!**

(c) Bump bonding

- Bump bonding defects $< 10^{-4}$ reported.

But some problems for the real ATLAS detector.

- Bump diameter can be $< 10\mu$,
  pitch can be $< 20\mu$
  (e.g. GEC Marconi)

Two types of bumps

	Indium	Solder
connection	pressure	fused
UBM *	simple	complicated
bump deposition	both sides	one side
Strength (4K bumps) (tension& sheer)	2.5 lb	10-14 lb (strong)
alignment required	1-2μ	$\sim 10\mu$ (self-aligning)
resistance/bump	1-2 Ω (poor)	2-3 $\mu\Omega$ (good)

* UBM = Under Bump Metalization

(d) Radiation Hardening

Radition damage effects:

a) Effective dopant creation
b) Leakage current increase
c) Threshold shift of MOS transistors

a) Effective dopant creation

Mostly p type

- Change in $V_{\text{depletion}}$ (e.g. increase)
  → high voltage breakdown, partial depletion
- Type conversion ($n \rightarrow p$) at high dose
  (OK for Belle)

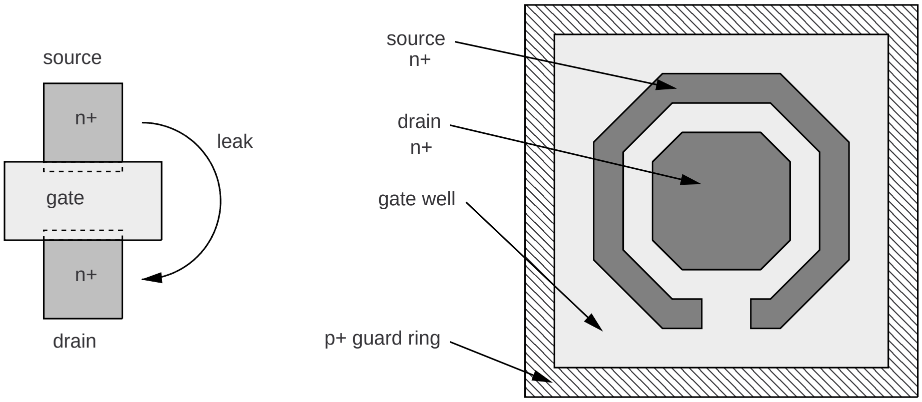
→ Thin sensor (low $V_{\text{depletion}}$), or
design such that it can stand high voltage
(e.g. guard rings at the edges of sensor)

b) Leakage current

1. source-drain leakage
2. inter-transistor leakage
3. detector bulk leakage current

Strategy:

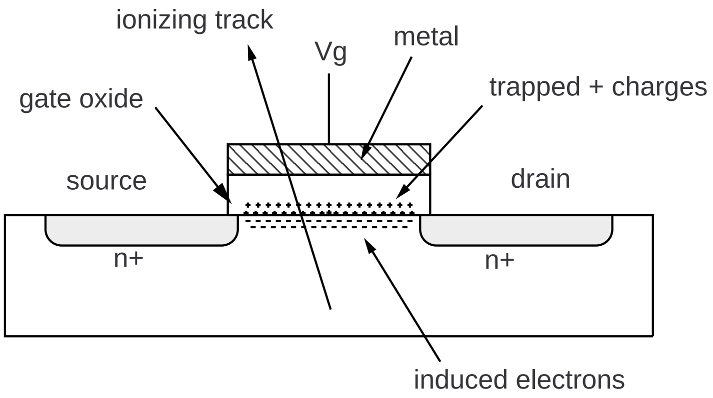
- Rad-hard design rules
  - ∗ Surround-gate design
  - ∗ p-stop around NMOS transistor



- current compensation for detector leakage (read-out electronics design)

c) Threshold shift of MOS transistor

Trapped positive ionization charges at gate-oxide
→ induces elctrons just below the gate.



$$\Delta V_{\text{th}} \propto \left\{ \begin{array}{l} t^2 \ (t < 10\,\text{nm}) \\ t^3 \ (t < 10\,\text{nm}) \end{array} \right.$$

t: gate thickness

Make the gate oxide thin:
← natural result of small scale processes.
(e.g. <u>commercial</u> IBM 0.25 μ process)

Hybrid vs Monolithic Summary

1. Monolithic pixel proven to work (32×32 array).

   Challenges:
   - larger detector
   - rad-hardness
   - **foundry !!**

2. Hybrid pixel design

   - heat $< 50\mu$W/pixel for LHC.
     Less for Belle → probably not a problem.
   - thickness $< 250\mu$ (sensor & read-out)
     being tested. 150μ total seems feasible.
   - bump bonding

     yield $> 99\%$:dummy test

     pad size can be $< 10\mu$, pitch can be $< 20\mu$
   - Rad-hardness of readout chip
     Deep subμ + rad.hard rules →
     30 MRad : IBM 0.25μ (ALICE)

→ **Pursue hybrid design**

Prototype Sensors

- Planar (conventional) pixel prototype
  - 300μm thick (no thinning)
  - 2 mm by 2 mm
    24 by 40 array, 50 by 100 μm^2 pixel
    (current SVD: 50 by 84 μm^2 readout pitch)
  - Design mostly complete (Chris Kenney)
  - Fabrication:
    By Chris Kenney at CIS (Stanford)
    #mask = 4-5

    Schedule
    Oct (B): mask ordered
    Oct (M): mask delivered
    Oct (E): fabrication begins
    (takes 1.5∼2 months)
    Dec (M): fabrication complete

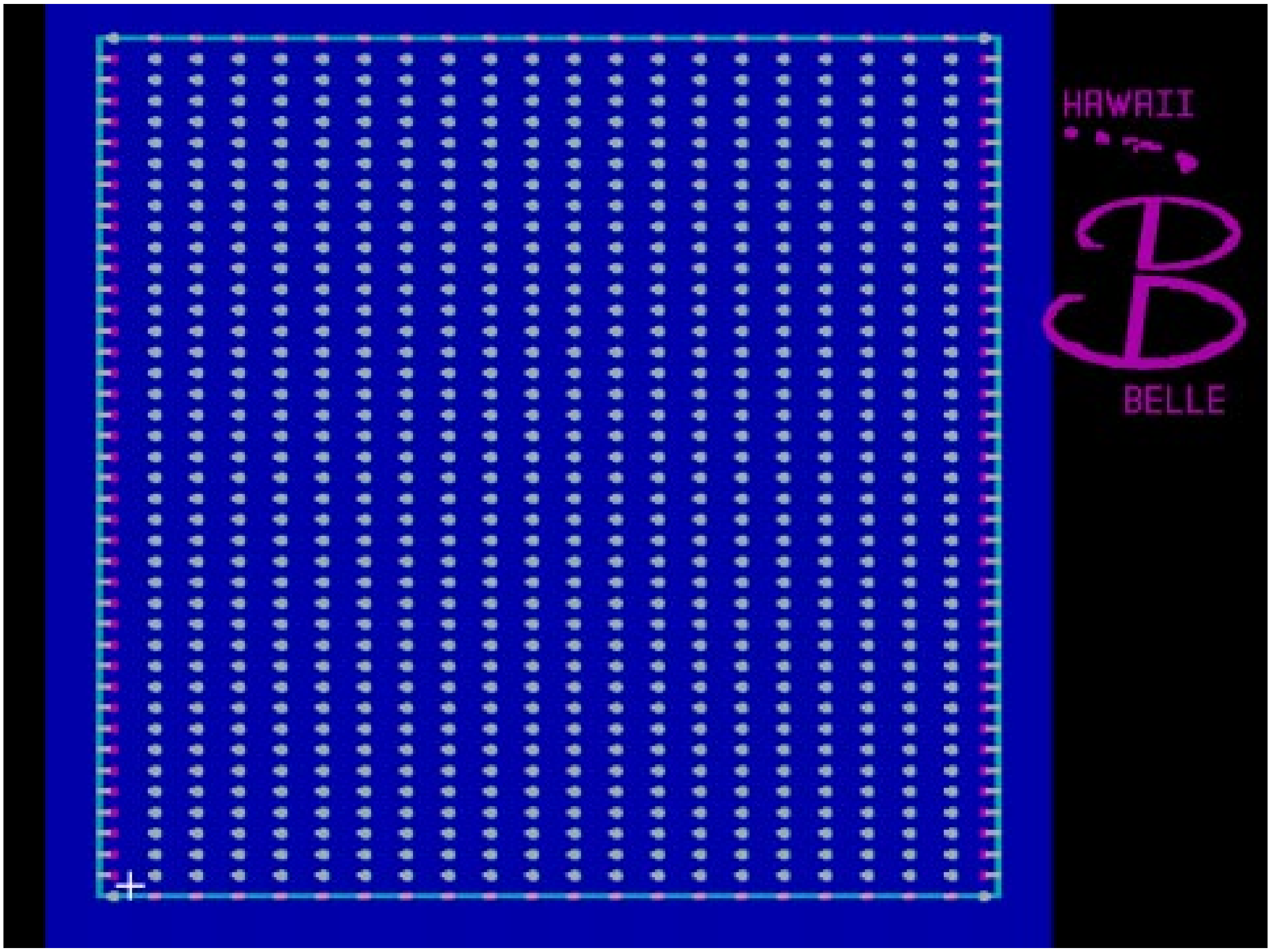
Prototype pixel sensor design

(Chris Kenney)

n^+ electrode

p^- substrate

p^+ backside



- 3D pixel sensor (Belle prototype)
  - 100μm thick
  - same size/pitch as the planar prototype
    (matched to Gary's readout chip)
  - fabrication:
    piggy-back on the ATLAS 3D sensor fabrication
    (simultaneous with the planar prototype above)

Bump Bonding Test

GEC Marconi (UK):
So far the only company to thin and bump bond.

Yamamoto visited the company in July, 1999.

- Submit to GEC Marconi: (Jan, 2000)
  - Dummy readout chips
  - Planar prototype sensors
  - Masks for UBM
- The readout chip will be thinned to $\sim 70\mu$m by GEC Marconi.
- Goal:
  - Bump bonding reliability test
    IR laser
    X-ray imaging
  - Measure bump bond capacitance

Vertexing R&D Personnel

- Software (Effect of bkg on vertexing/physics)
  - Karim Trabelsi (arr. Nov 99) and friends.
- Sensor/electronics testing/coordination
  - Gianluca Alimonti (arr. Jan 1, 2000
    - pending INFN approval) and friends.
- Sensor design/fabrication
  - Chris Kenney/Sherwood Parker and friends.
- Electronics/Integraqted Circuits
  - Gary Varner and friends.
- Mechanical design
  - Mark Rosen and friends.
- Beam background study
  - Coordination: Tom Browder/Hitoshi Yamamoto
    → Synchrotron radiation: Sanjay Swain
    → Beam Gas: Hulya Guler
    ······ and friends.

Committment from Belle

US-Japan: $61K to Hawaii this year
for Belle pixel R&D.

OK for now, but as we will start fabrication of more prototype sensors, submission of readout electronics and hybridization, more funds will be needed.

Need for next year

Sensor fabrication (CIS fee, wafer, thinning)	15K
Readout Chip	90K
Other electronics	10K
Hybridization	60K
total	175 K